Cisco Silicon One and IOS XE Architecture and Innovation

Cisco Catalyst 9000 Series

Shawn Wargo
Principal TME

Session ID: BRKARC-2092

Cisco Webex App

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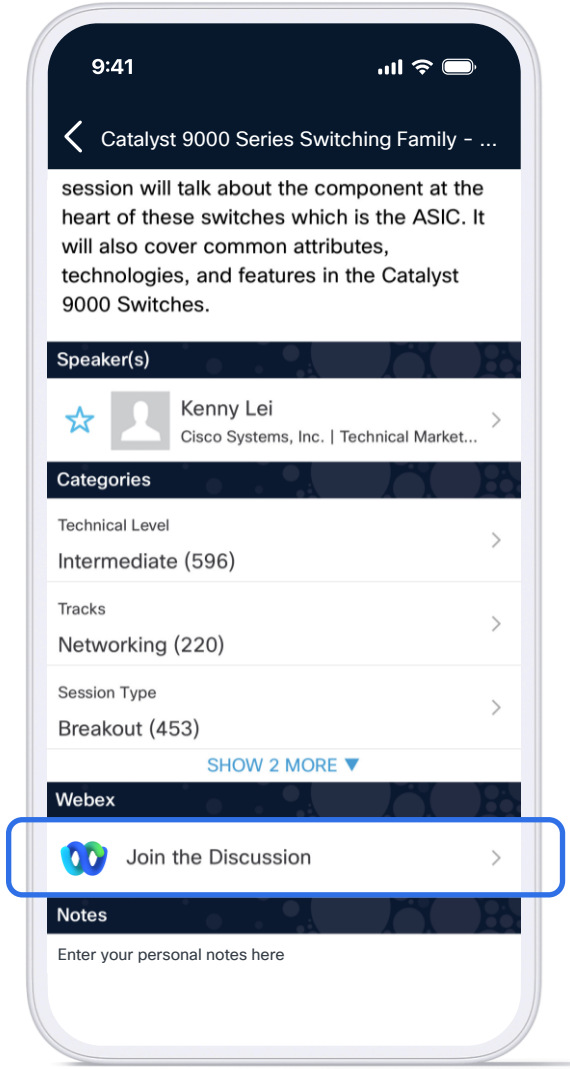

https://ciscolive.ciscoevents.com/
ciscolivebot/**#BRKARC-2092**

Who am I?

I'm a **Principal Engineer of Technical Marketing** (Principal TME) for Cisco Enterprise 'Network Experience' (NX) Product Management team. I've been with Cisco **since 1999**.

I mainly focus on **Enterprise Switching & Routing** technology areas, with a special emphasis on '**next generation' Hardware & Software** products and solutions.

As a Principal TME - I'm currently working on the next generation of **Cisco Switching, Wireless & Routing** products, and solutions like Software-Defined Access (SDA) & Cisco UNX.

#HighBitRate

Shawn Wargo
Principal TME

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@shawn_wargo

Why BRKARC-2092?

Learn about ASICs & IOSXE in one session

BRKARC-2090

BRKARC-2091

Cisco ASICs - What this session is NOT about

This session is **NOT** a detailed ASIC "deep-dive"!

- **Level 2** - Intermediate
- **Limited Time** (only 45 minutes)

This session also does not go into detail about the (many) IOS XE features

Goal is to *introduce* & *familiarize* you - so you want to *learn more* ☺

Other **Related Sessions**:

- **BRKARC-1011** - Cisco Silicon One: Innovation at Speed and Scale
- **BRKARC-2093** - Cisco Innovations in Silicon & Software
- **BRKARC-2098** - Catalyst 9000 Series Switching Family - Access
- **BRKARC-2099** - Catalyst 9000 Series Switching Family - Core and Distribution
- **BRKARC-2668** - Campus Switching Architecture for Future Proofed Workspaces

Cisco IOS XE – What this session is NOT about

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Other **Related Sessions**:

- **BRKENS-2004** – Catalyst 9000 IOS XE Innovations
- **BRKARC-2098** – Catalyst 9000 Series Switching Family – Access
- **BRKARC-2099** – Catalyst 9000 Series Switching Family – Core and Distribution
- **DEVNET-1110** – Modern approaches for IOS XE network device management on Cat9k

Cisco 9000 Series – Common Building Blocks

Multi-Core x86 CPU

Application Hosting
Secure Containers

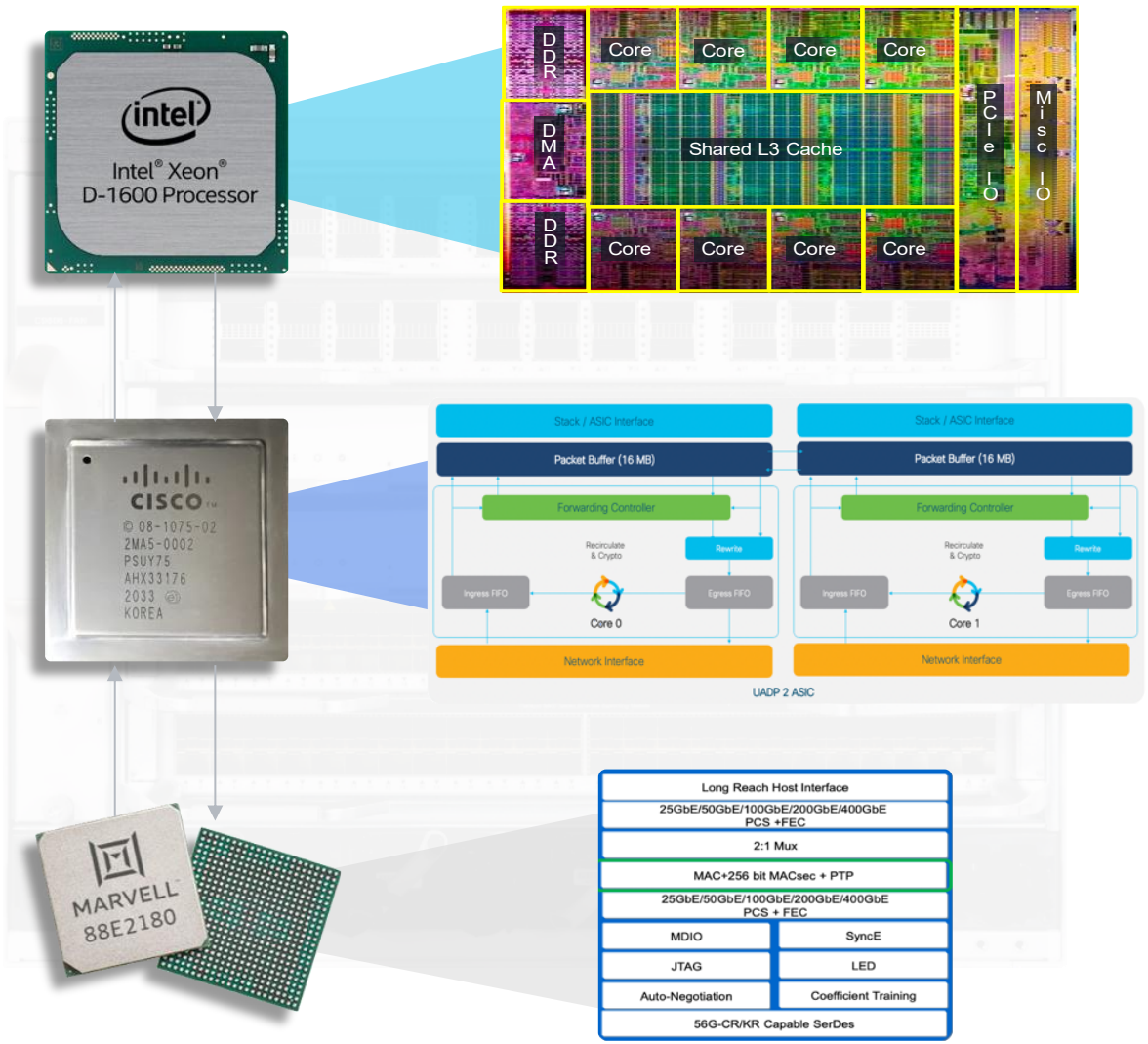
Cisco IOS XE®

Model-Driven APIs
Modular Patching

Cisco UADP & Silicon One™

Programmable Pipeline
Flexible Tables

Software vs. Hardware



CPU/DRAM

Where the OS "software" runs. Includes control-plane, data-plane and system-management functions.

- **OS layer** – IOSXE (IOSd) and Features, etc.
- **System layer** – FMAN, CMAN, IOMD, FED, etc.

ASIC(s)

Where the "hardware" processing of traffic & services runs. Uses forwarding and state tables programmed by the software.

- **Forwarding** – L2, L3, ECMP, Encap, etc.
- **Services** – ACLs, QoS, Analytics, Encryption, etc.

Stub/PHY(s)

Transforms electrical and optical signals, splits or combines signals, and other various "physical" layer functions, such as encryption and timestamping.

What's New?

CiscoLive 2025 - San Diego

NEW

New Cisco C9000 Smart Switch Series

Campus-Driven S1 NPU 2.0 ASICs

A100 (C9350) and K100, E100 (C9610-SUP3)

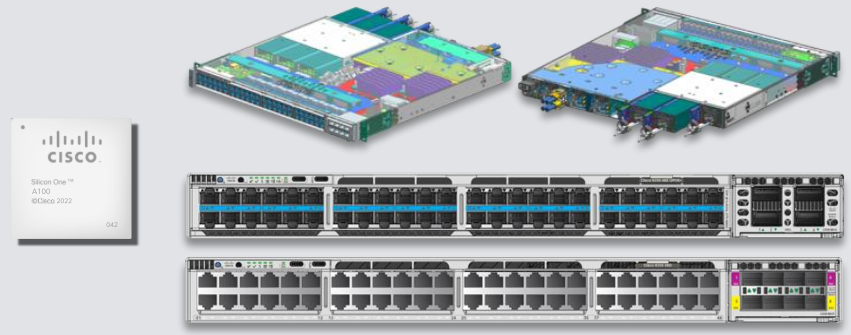
AI-Ready X86 & DDR5 CPU & DRAM

Intel RPL I3 (C9350) and Intel ICX-D (C9610-SUP3)

Cloud-Native IOS XE 3.0 Software

UNX, Multi-Mode, Programmability, HyperStack, SD-Access, Smart Power

C9350 Series Smart Switches



C9610 Series Smart Switches

Cisco UADP & Silicon One

ASIC Architecture & Innovations
Cisco C9000 Series

Agenda

01 Why do we need ASICs

02 Flexible ASICs & Cisco UADP

03 Cisco Silicon One ASICs

04 Cisco 9000 Smart Switches

05 A Glimpse into the Future

Catalyst 9000 Series – Common Building Blocks

Multi-Core x86

Application Hosting
Secure Containers

Cisco IOS XE®

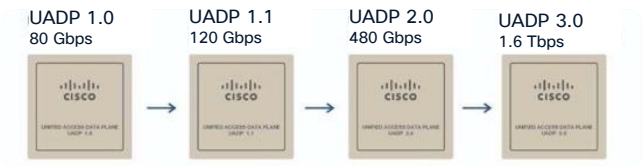
Model-Driven APIs
Modular Patching

Cisco UADP & Silicon One™

Programmable Pipeline
Flexible Tables

Custom ASICs – Programmable Silicon

Cisco Unified Access Data-Plane (UADP)



Cisco Silicon One™

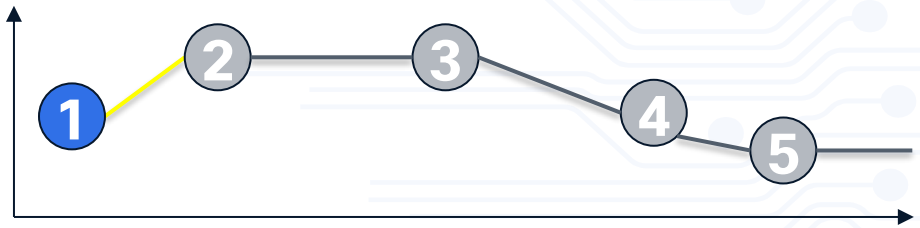
Flexible Pipelines
Investment Protection

Adaptable Tables
Universal Deployment

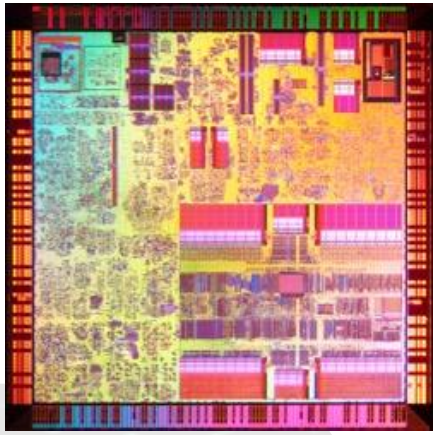
Scalable Resources
Enhanced Scale and Buffering

Flexible & Programmable ASICs – Adapt to New Technologies

Why do we need ASICs



What is an ASIC?



Application Specific Integrated Circuit (ASIC) is a silicon microchip designed for a specific task ...

... rather than '*general-purpose*' processing in a **CPU**.

Why not use CPUs?

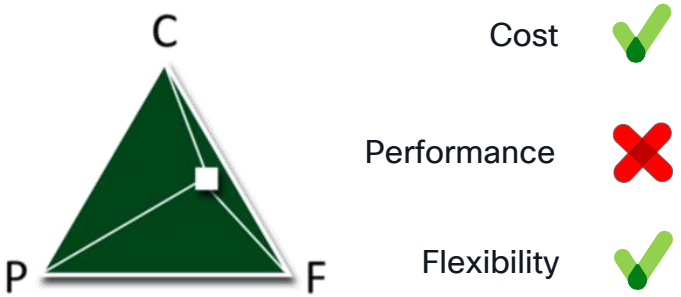
CPUs are **Flexible** but **Slow**

A ‘general-purpose’ CPU may be fast at running random-access applications, on a laptop or server, but **processing and forwarding ‘network traffic’** is a different matter.

Network traffic requires **constant searching of large memory** tables (e.g. L2 tables for MAC addresses, L3 tables for IP routes, L4 ACLs for Security and QoS, etc.)

In a CPU – there are **limited data paths** and tables are held in **off-chip memories** (e.g. DRAM) that can incur significant performance penalties for frequent access.

Remember, this is **Millions** – **Billions** of packets per second



Multi-Core ASIC Design

Combining multiple Processors in same ASIC

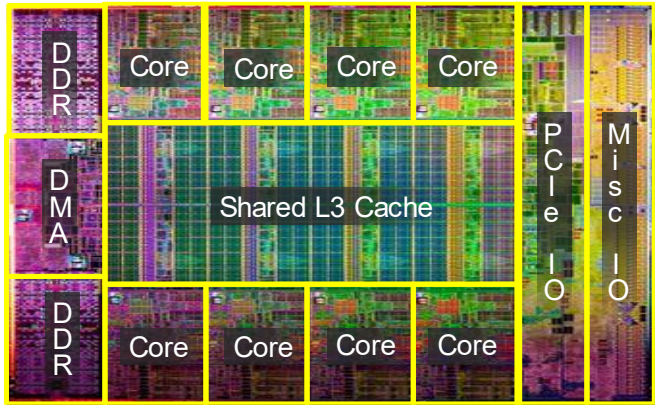
Multiple-Core processors have been used in personal computers since the mid 1990s.
So, while the concept is not new – it's good to briefly revisit.

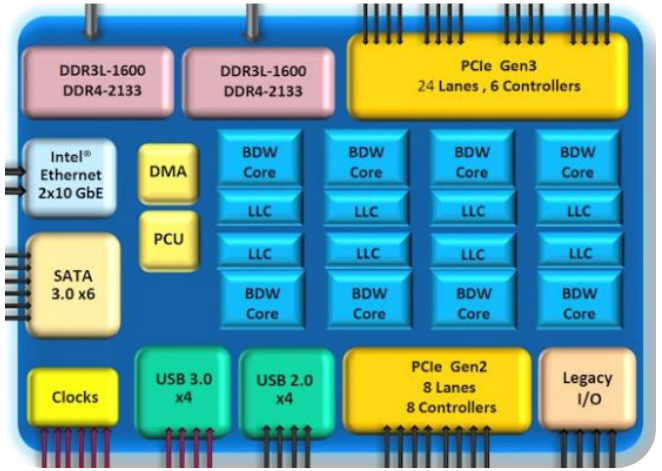
Multi-Core design addresses the physical **limitations of per-processor clock speed** (e.g. how effectively can they be cooled), by **load-sharing across multiple processors**.

However – there are practical (physical) limits to **how many cores yield improvements**, and cores must **share all external co[illegible]ents**.

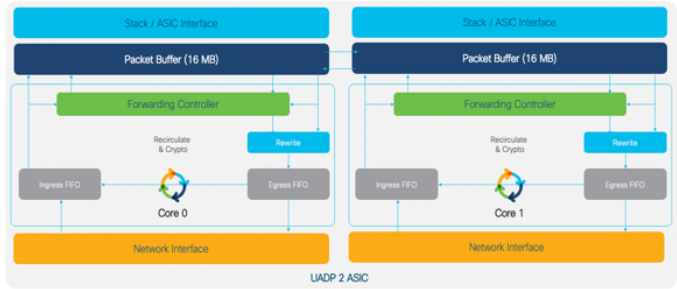
TIP Cisco UADP & QFP are examples of using multiple Processor Cores to boost overall ASIC performance

Intel Xeon 8-Core

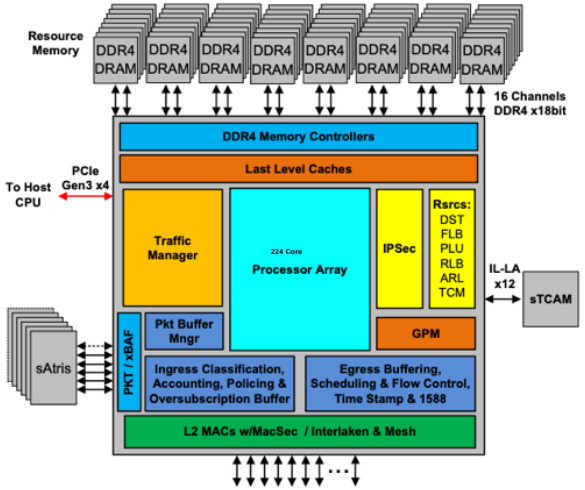




UADP (C9K)



QFP (ASR/C8K)



Why not use FPGAs?

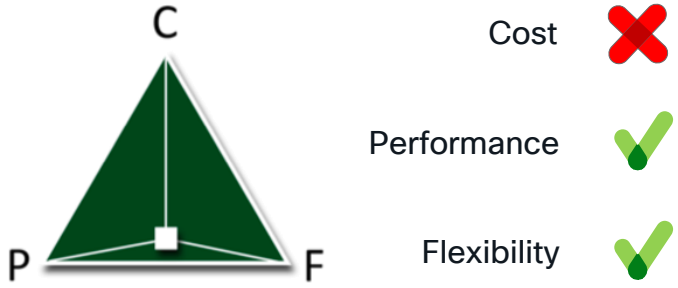
FPGAs are
Flexible but **Expensive**

FPGAs do provide a lot of design flexibility, but they can be **very expensive to develop and support**. They are not built for any specific task and must be reprogrammed for each new task.

FPGAs also **have little or no onboard memory**, requiring other components to provide memory access.

These limits generally relegate FPGAs to a "**special-purpose**" role in most network devices. FPGAs are most often used to augment other ASICs, for the "**one extra feature**" the primary processor does not have.

FPGAs typically **cost far more (10X) more** than an equal ASIC



Field Programmable Gate Arrays

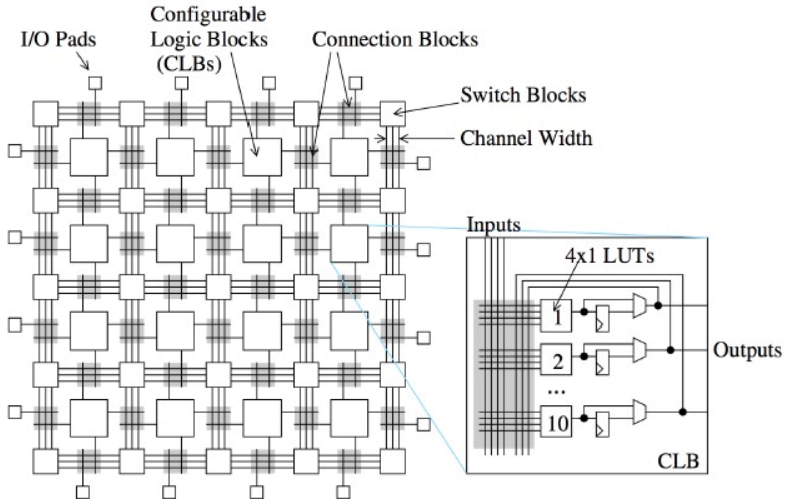
FPGAs can be re-programmed after Manufacturing

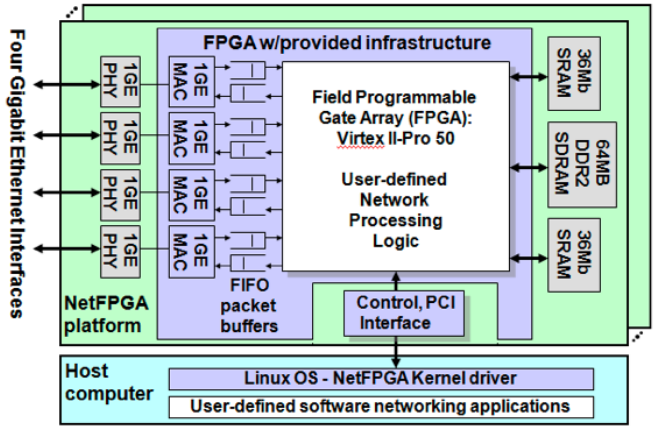
As the name suggests, **an FPGA is an integrated circuit** (like an ASIC) with **sets of logic gates and memories** (a gate array), which a **user can re-program** (in the field), after silicon manufacturing, to perform one or more logical operations.

With a fixed ASIC, the microchip is fully baked. It can't be reprogrammed; you get what you get. The software can be deleted or replaced, but the hardware is unchanged.

With an FPGA, there are **no predefined hardware circuits**. The user programs the circuits. The programming can be a single, simple logic gate (e.g. just an AND or OR function), or it can involve multiple complex functions that, together, act as a complete multi-core processor.

You might use an FPGA if you may need to make changes at the chip-level during development (e.g. prototypes), or even to augment another ASIC, to add a new feature.

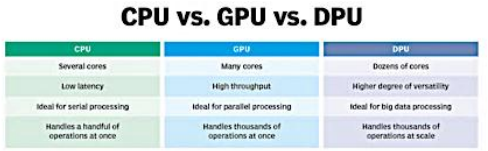


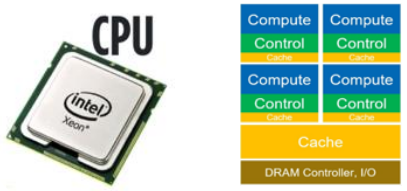


intel.com/content/dam/www/programmable/us/en/pdfs/literature/misc/fpgas_for_dummies_ebook.pdf

CPU vs. GPU vs. DPU (& SOC)

Normalizing Terminology – Data Processors





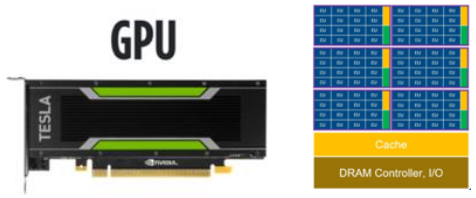
Central Processing Unit

*A **central processing unit (CPU)** is commonly referred to as the 'brain' of a computer. A CPU is essential to all modern computing systems and may use one or multiple processing cores.*

*A CPU **performs all general-purpose computations centrally**, including low-level Operating System (OS) infrastructure, as well as random Application software programs.*

Thus, the system performance is the sum of all software programs running on the CPU.

Major Vendors: Intel & AMD



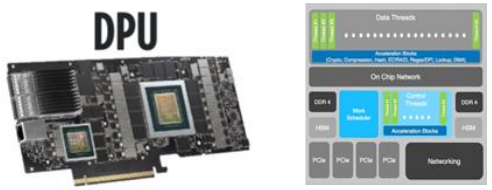
Graphics Processing Unit

*A **graphics processing unit (GPU)** was originally designed to offload the computer CPU for **video graphics processing**.*

A GPU has many smaller, but specialized cores. These cores deliver massive performance by working together and dividing processing tasks across many cores simultaneously (in parallel).

*A GPU **excels at highly parallel tasks** like rendering visuals, manipulating data during content creation, and computing results in intensive AI workloads.*

Major Vendors: NVIDIA & AMD



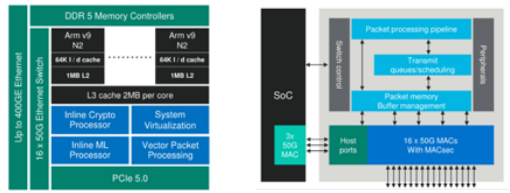
Data Processing Unit

*A **data processing unit (DPU)** was originally designed to offload the computer CPU for **network processing** (NIC). This gave it the earlier term: SmartNIC.*

A DPU is focused on moving and processing data within a local network (e.g. data center).

*DPU is a new class that combines elements of both CPU & GPU while adding **acceleration engines for unique functionalities** like network path processing, network security, load-balancing and storage networking.*

Major Vendors: Marvell, Mellanox



System on Chip

*A system on chip is a combination of all three (**CPU+GPU+DPU**) in a single integrated system.*

1. ***Multi-Core CPU**:*
   A standard, high-performance, programmable, multi-core CPU (often based on ARM architecture).
2. ***Programmable Micro-Engines**:*
   To boost performance for apps like AI and Machine Learning, security, physical media, crypto and storage.
3. ***High-Performance NIC**:*
   This ensures efficient buffering and data transfer to GPUs and CPUs at the network's speed.

Also check out
Tensor Processing Unit (TPU)

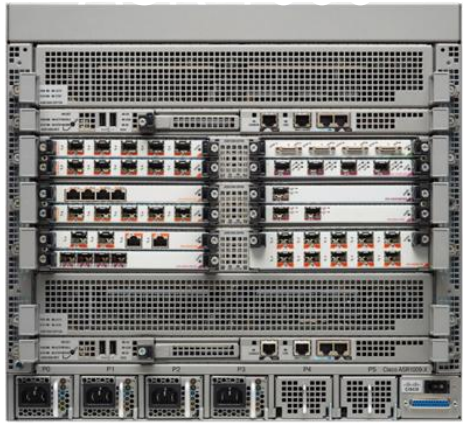
cisco

Hardware vs. Software Data-Plane

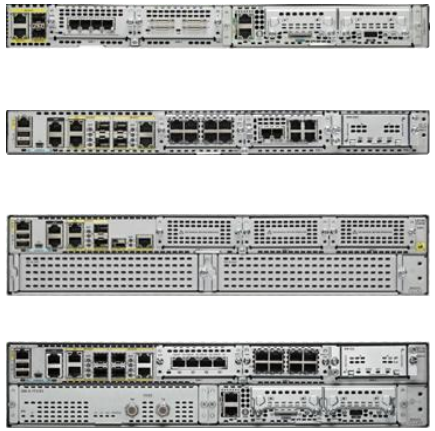
ASIC-based vs. CPU-based Packet Forwarding

S1/UADP

QFP



X86/ARM



Hardware-Based (ASIC)

PROs

- **High Throughput**
- Gbps – Tbps
- High Port Density
- HW-based Services
- Lower COGs

CONs

- **Less Flexible**
- PI + PD Development
- Longer Dev & Test
- Scale limited by HW
- Limited Services

Software-Based (CPU)

PROs

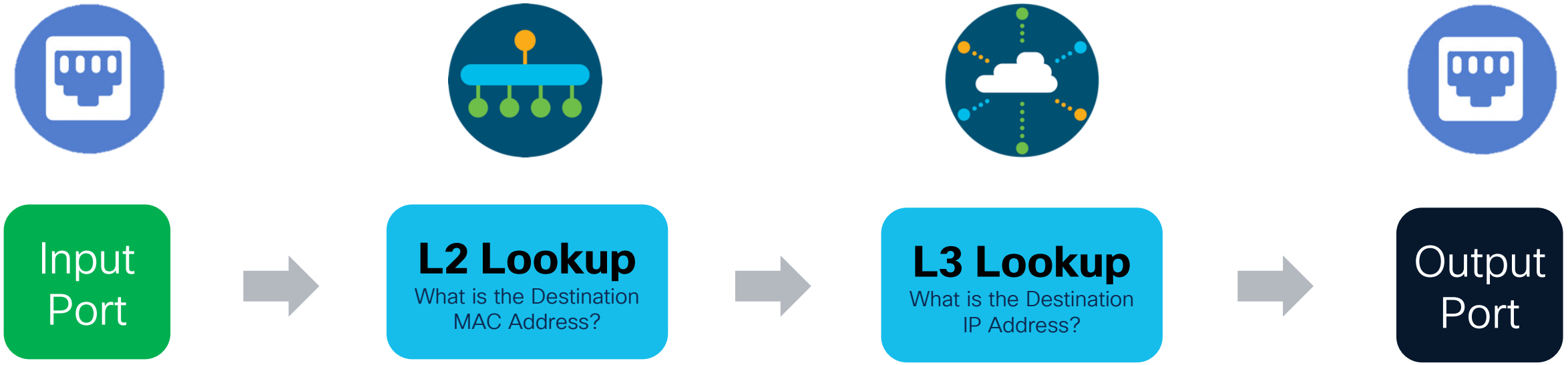
- **More Flexible**
- PI Only Development
- Faster Dev & Test
- Scale limited by CPU
- Lots of Services

CONs

- **Low Throughput**
- Mbps – Gbps
- Low Port Density
- SW-based Services
- Higher COGs

What does an ASIC do?

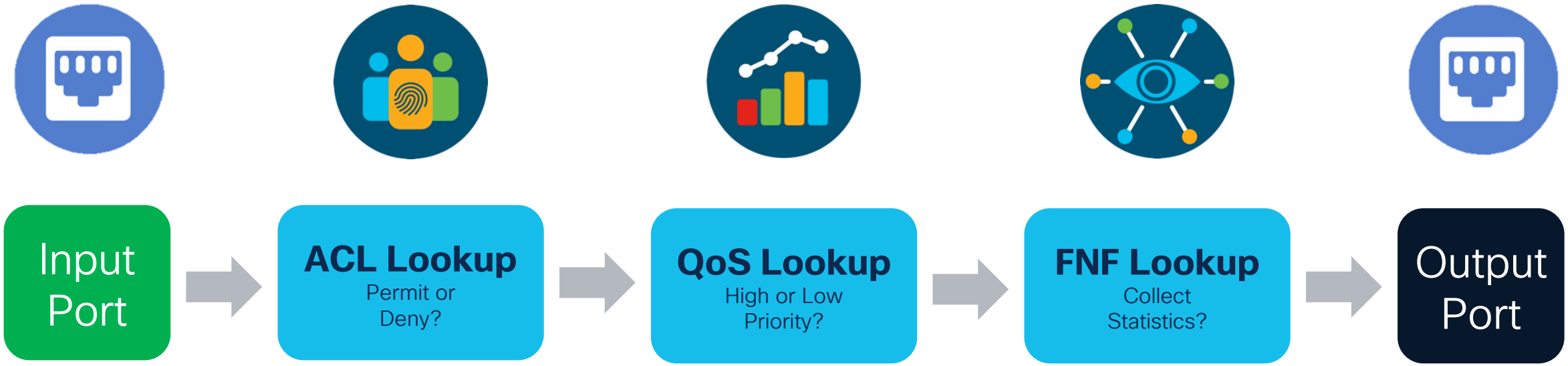
ASICs are fundamental to network devices



Modern processing speeds are **Terabits per second (Tbps)**

What does an ASIC do?

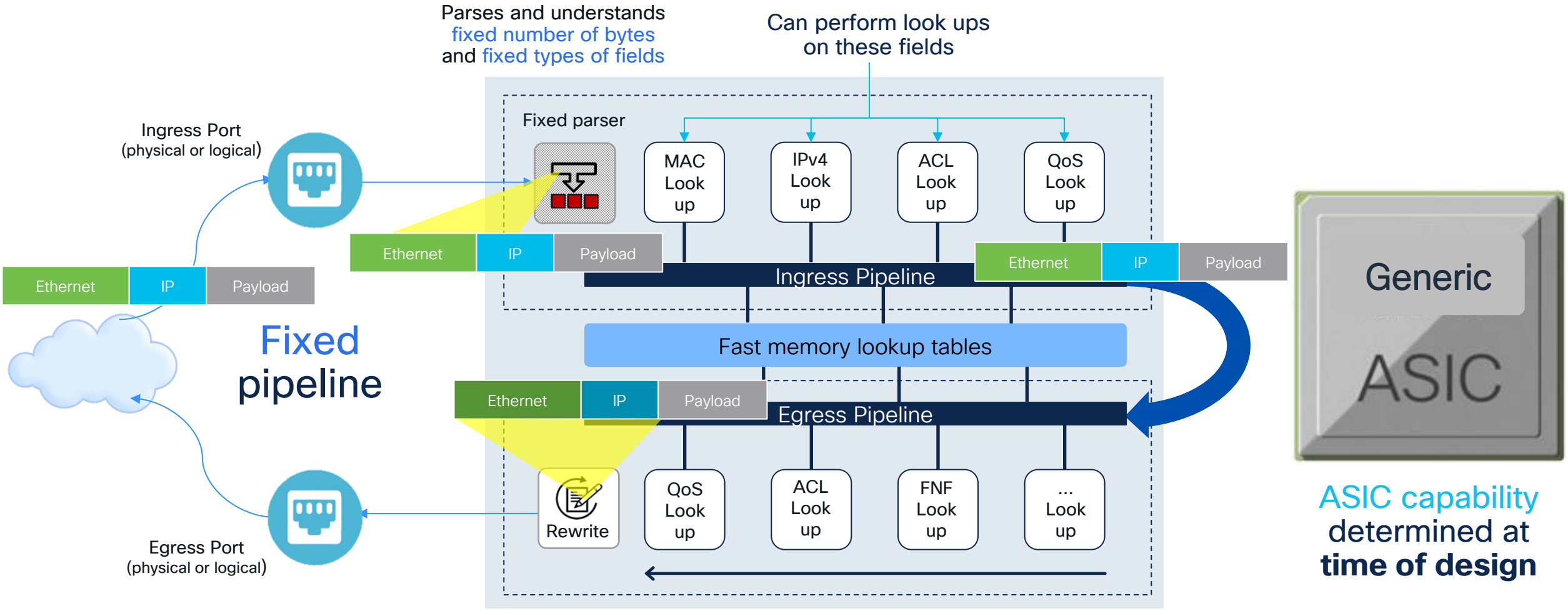
ASICs are fundamental to network devices

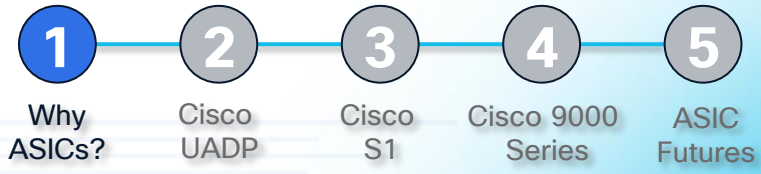


Common services are **Access Control**, **Quality of Service** and **Flow Analytics**

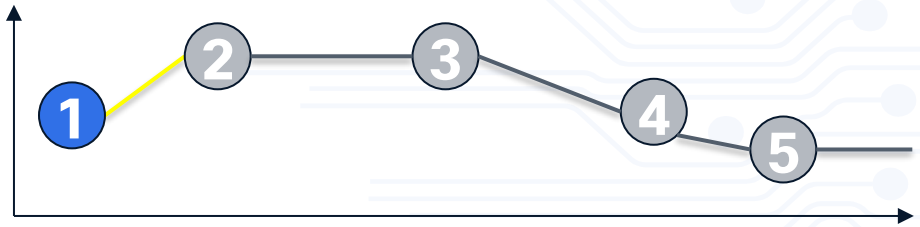
The Past – Fixed Network ASICs

Fixed Processing Pipeline





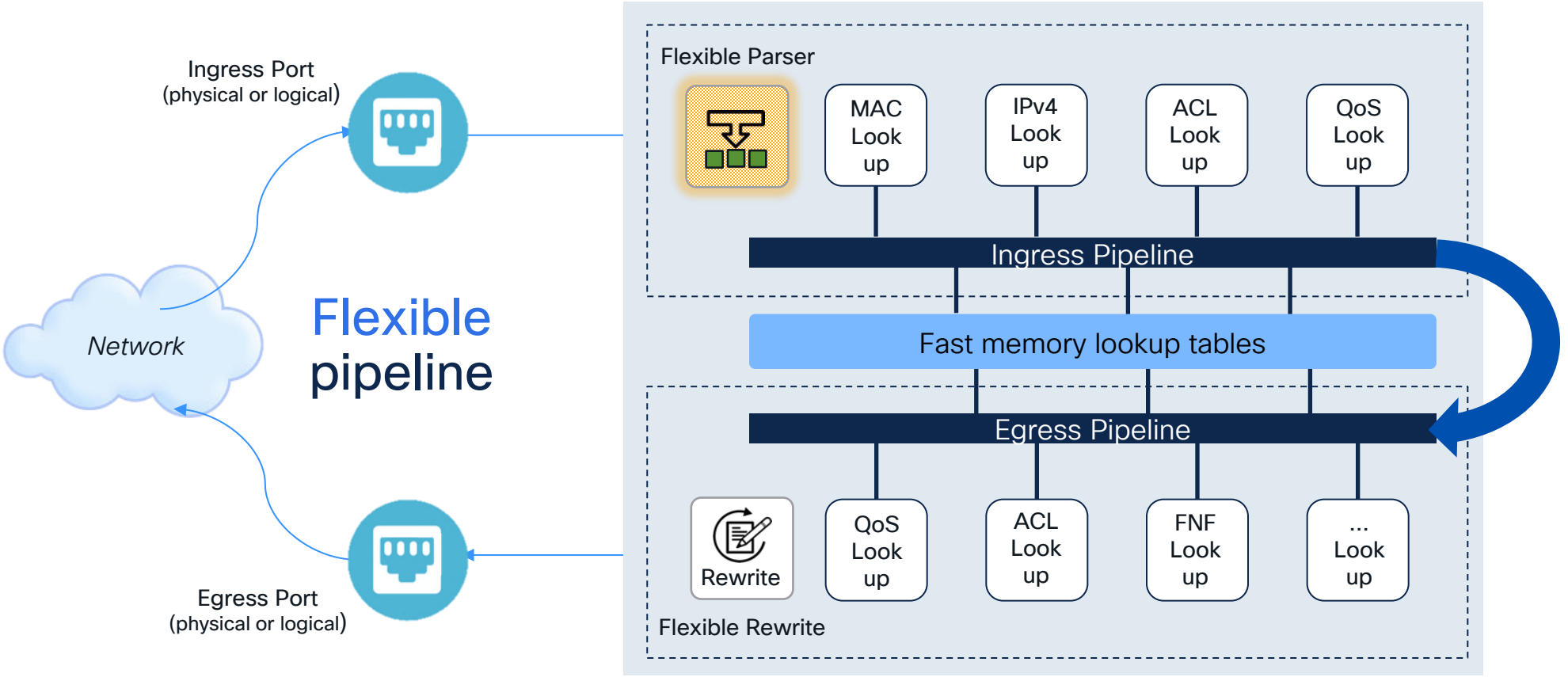
Flexible ASICs for Enterprise Switching



Programmable Network ASICs

Flexible Parsing

Parses and understands
multiple programmable headers
with flexible field definitions



Flexible Parsing

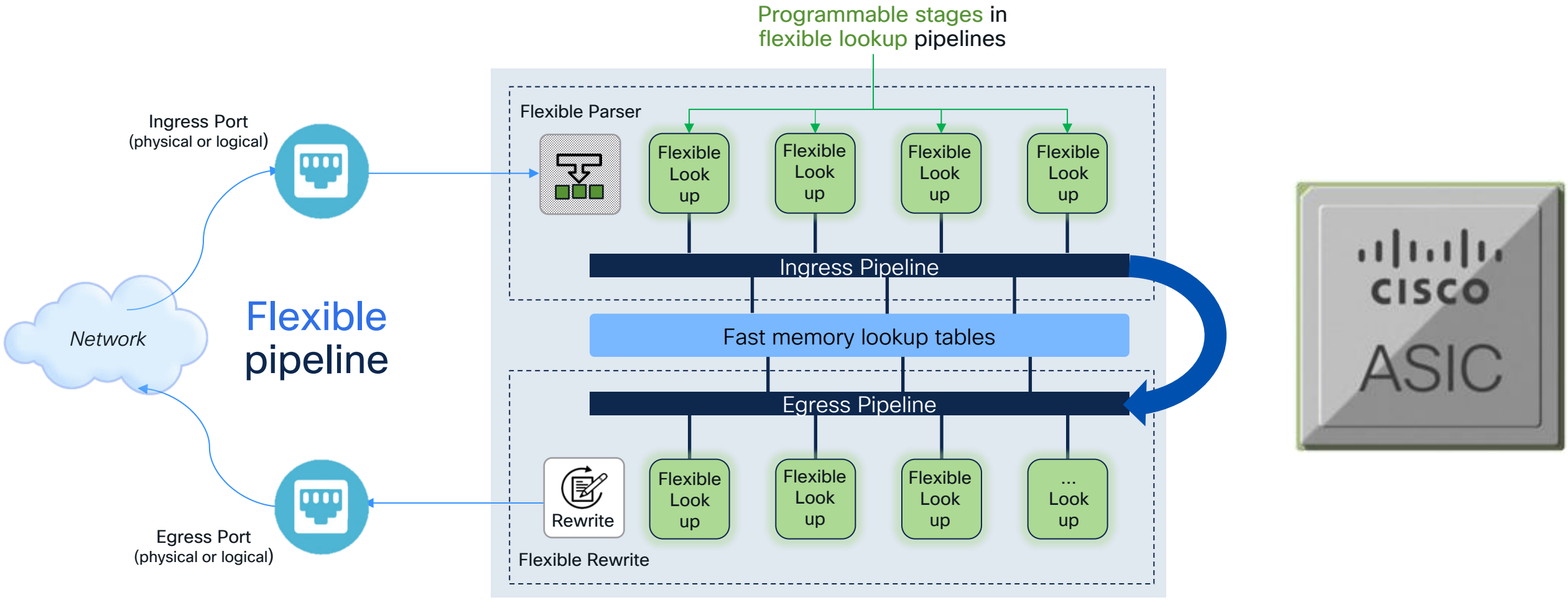
Look deep into the packet header,
with **programmable field parsing**

Programmable Network ASICs

Flexible Lookups

Flexible Lookups

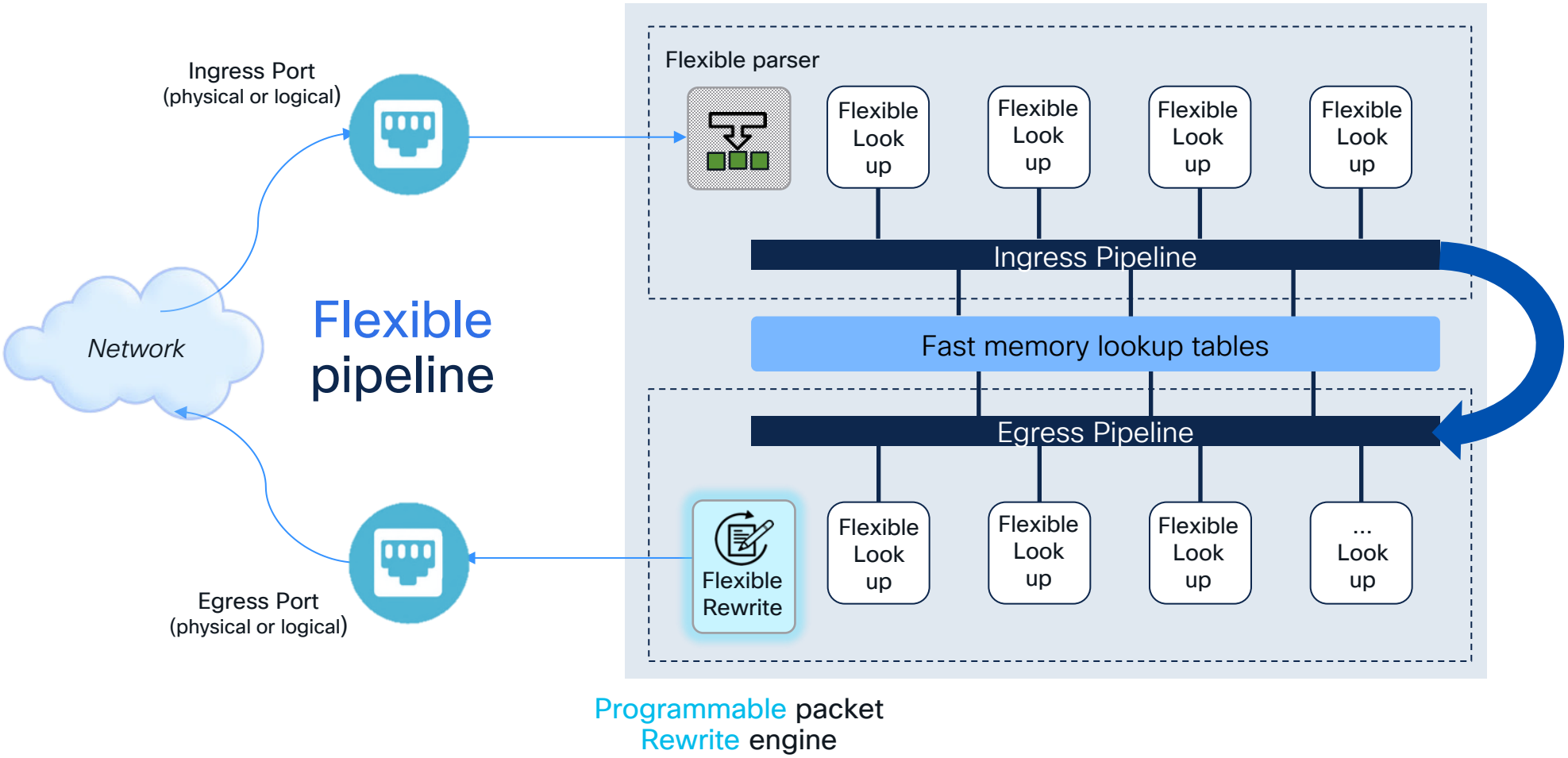
Multi-stage packet handling, with **flexible packet lookups** at every step



Programmable Network ASICs

Flexible Rewrites

Flexible Rewrites
Flexible packet handling and forwarding,
with a programmable packet rewrite

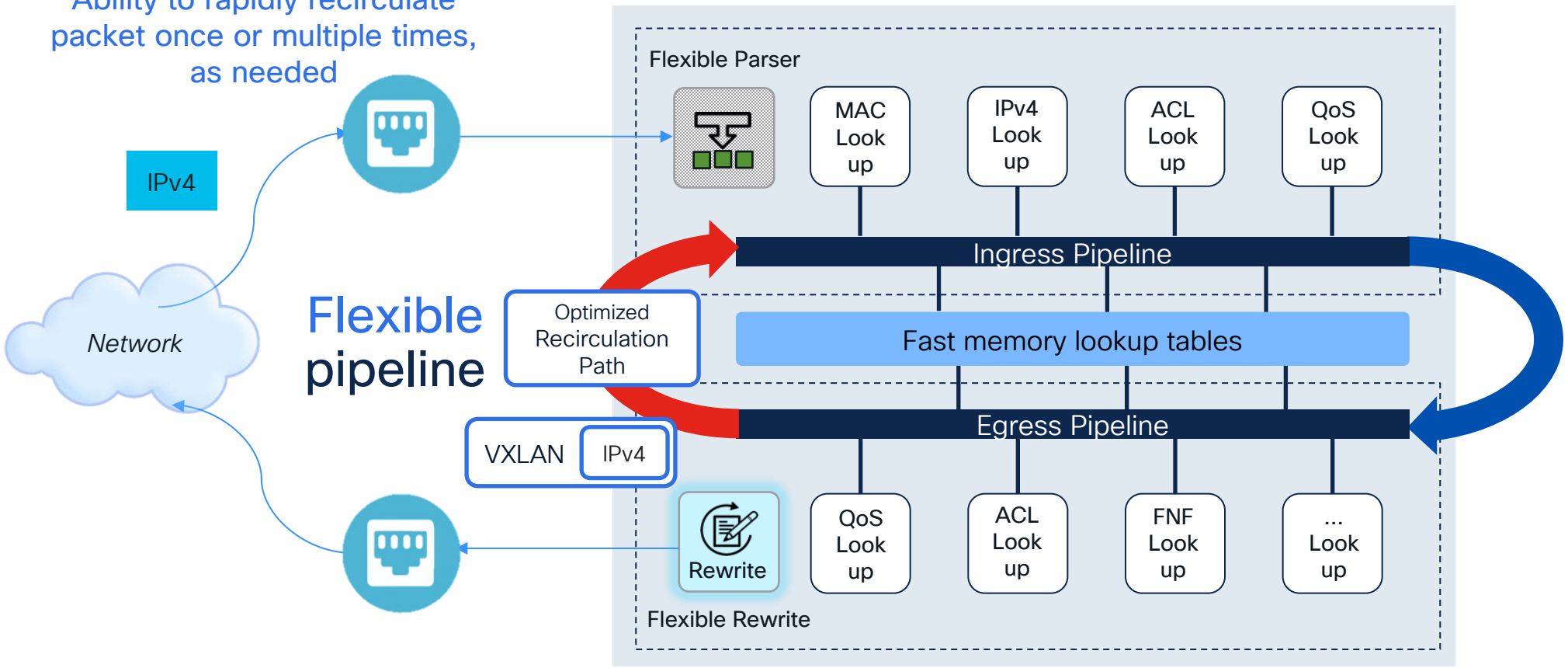


Programmable packet
Rewrite engine

Programmable Network ASICs

Optimized Recirculation

Ability to rapidly recirculate packet once or multiple times, as needed

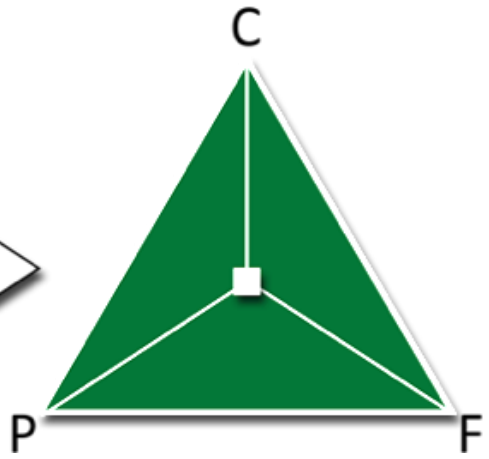


Optimized Recirculation

Highly **optimized recirc path** for packet header addition / removal / forwarding

Programmable Network ASICs

Balancing Cost, Performance & Flexibility



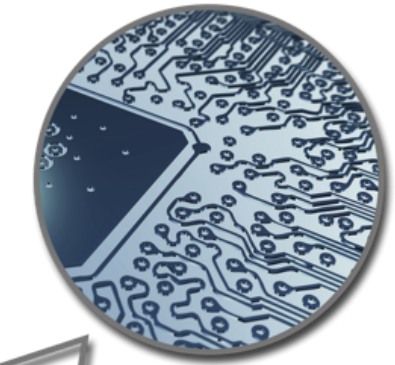
Cost

Performance

Flexibility

ASIC
Engineer

Microcode
Update



New ASIC
Functionality

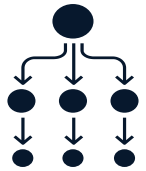
cisco

Creating Custom ASICs

From Definition to Deployment







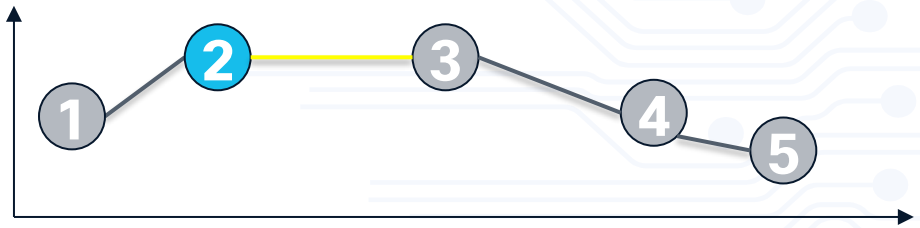
Marketing requirements | Architecture | RTL design | Synthesis | Floor planning | Fabrication | NEW

3 to 5 years

Building a new Custom ASIC takes a lot of Time and Money

Yes... we are already building the 'Next Generation'

Cisco UADP for Enterprise Switching



Cisco Unified Access Data-Plane (UADP®)

Common ASIC Architecture for Campus Switching Access, Distribution & Core

community.cisco.com/t5/networking-blogs/uadp-the-powerhouse-of-catalyst-9000-family/ba-p/3764605

UADP 2.0m

120 Gbps

16nm FinFET
1 Core + ARM CPU

UADP 2.0/XL

240 Gbps

28nm FinFET
2 Core

UADP 2.0sec

480 Gbps

16nm FinFET
1 Core2 + SEC

UADP 3.0

1.6 Tbps

16nm FinFET
2 Core

UADP 3.0sec

1.6 Tbps

16nm FinFET
2 Core + SEC

- **Multiple generations and formats, same architecture**
- **Rich flexible forwarding & services memories**
- **First fully programmable microcode network silicon**
- **Multiple functions: system-on-chip or line-card**
- **Multiple form factors: fixed or modular**
- **Multiple places: Access, Distribution and Core**

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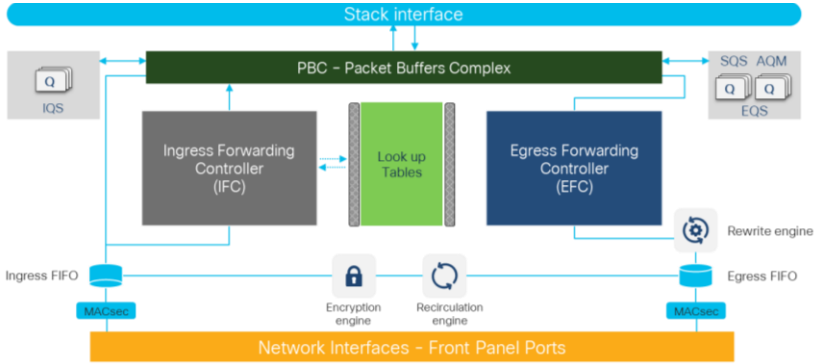
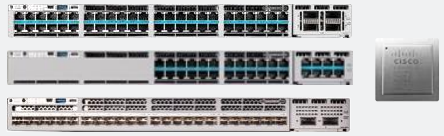
Catalyst 9000 with UADP

The industry's first Programmable Campus ASIC Family



Catalyst 9200CX
UADP 2.0 mini

Catalyst 9300X/LM
UADP 2.0sec



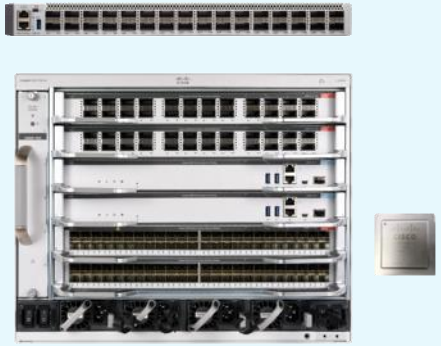
Catalyst 9400X-SUP2
UADP 3.0sec

Catalyst 9200/L
UADP 2.0 mini

Catalyst 9300/L
UADP 2.0

Catalyst 9400-SUP1 & 9500
UADP 2.0XL

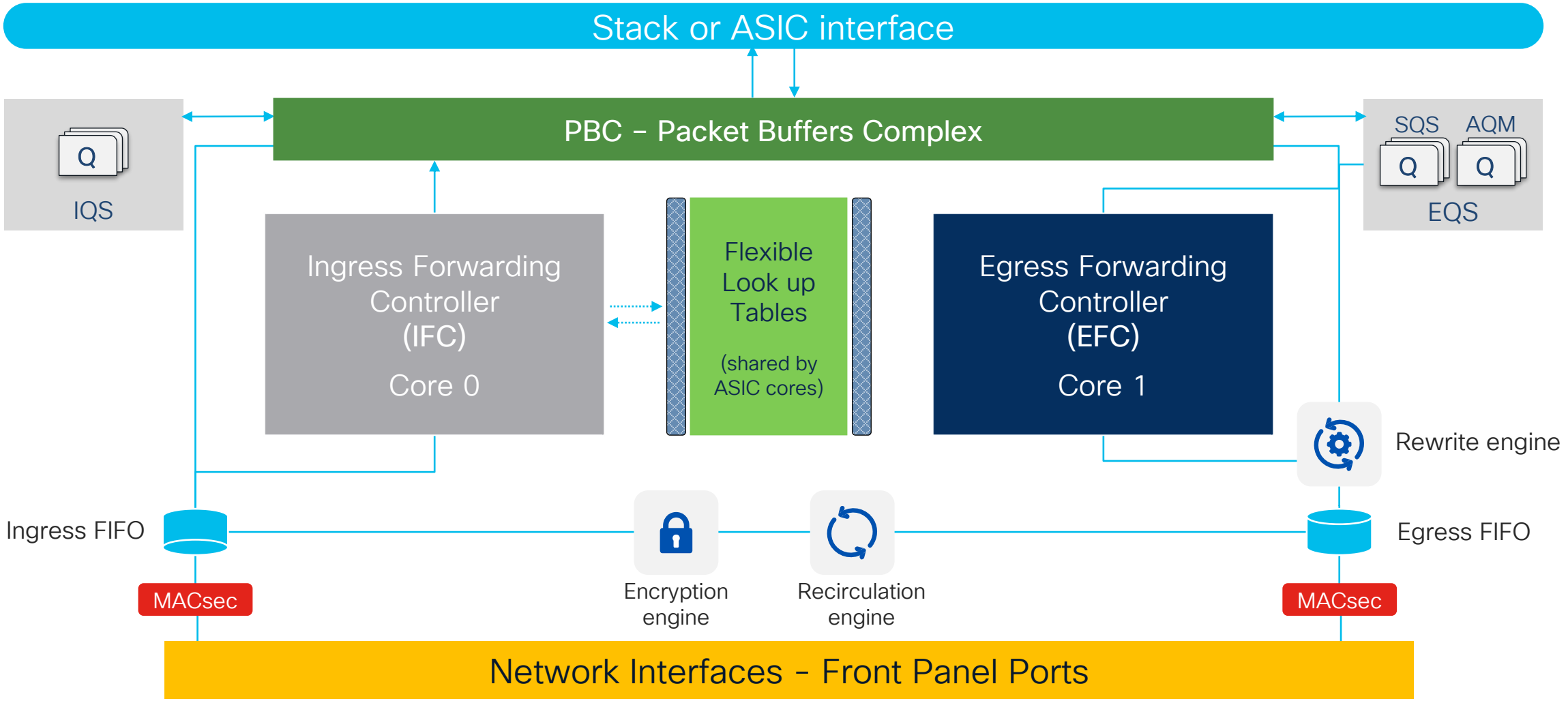
Catalyst 9500(H) & 9600-SUP1
UADP 3.0



Cisco UADP ASICs

ASIC Architecture & Block Diagram

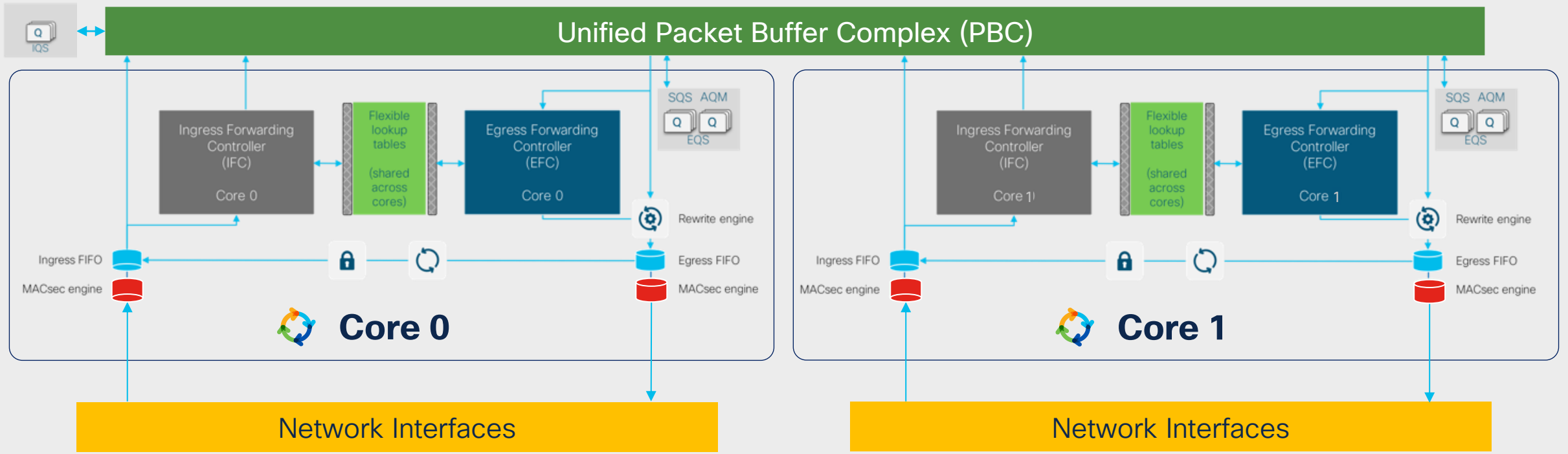
up to 1 BILLION times per second!



Cisco UADP – Dual Cores

Multiple ASIC Cores & Unified Packet Buffers

Each ASIC “Core” services a certain number of front-panel ports



Cisco UADP – Flexible Lookups

Programmable Ingress and Egress Processing Stages

Final decision on packet's future

15 Ingress Programmable stages

IGR

Stage 15
Stage ...
Stage ...
Stage 2
Stage 1

Flex parser

2 lookups per stage

Flex parser 256 B

Flexible lookup tables

ACL Table	ACL Table	ACL Table	ACL Table
LPM Table	LPM Table	LPM Table	LPM Table
LPM Table	LPM Table	LPM Table	LPM Table
LEM Table	LEM Table	LEM Table	LEM Table
LEM Table	LEM Table	LEM Table	LEM Table

Flex parser 256 B

Flex parser

Stage 1
Stage 2
Stage ...
Stage ...
Stage 8

EGR

8 Egress Programmable stages

FORWARD or RECIRCULATE

Final decision on packet's future

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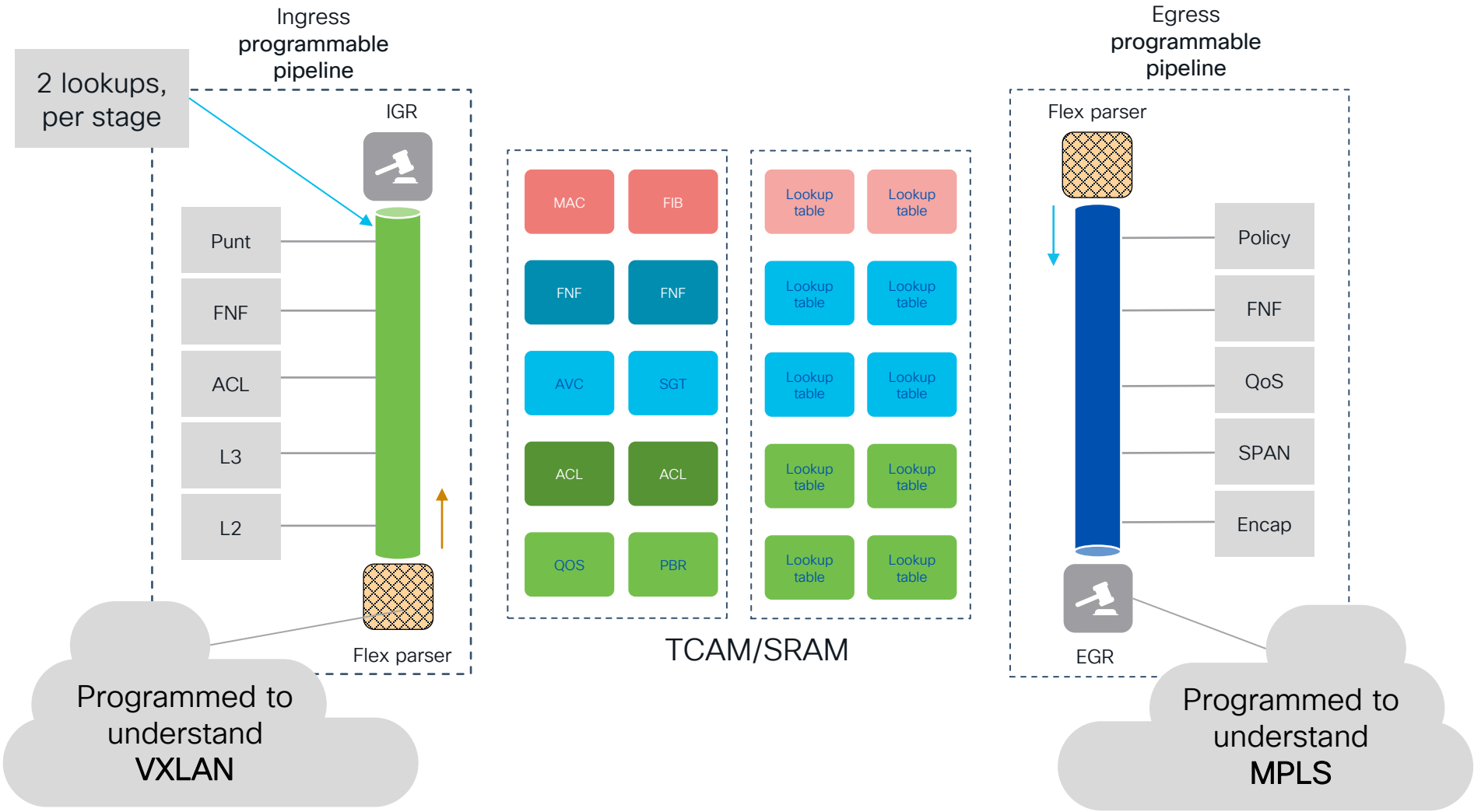
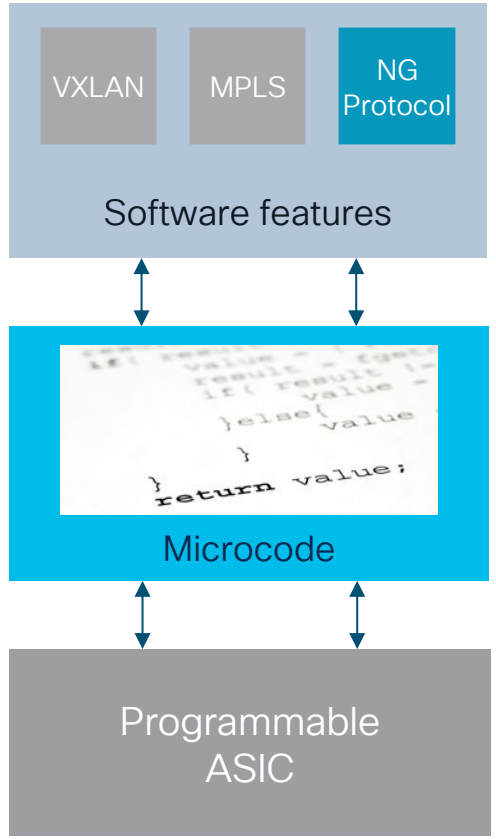
Cisco UADP – Microcode

ASIC Microcode (NPL/SDK) can be upgraded to add new features





Cisco UADP – Flexible Tables

Customizable ASIC tables for universal deployment flexibility

SRAM/TCAM

- 64K
- 256K
- 32K
- 48K
- 16K
- 8K
- 4K

- MAC
- IPv4/v6
- Unicast
- Multicast
- NetFlow
- ACL
- SGACL
- QoS
- NAT
- SPAN

Flexible ASIC templates

Access template	Core template	Distribution template	NAT template
Layer 2 and Client scale	Layer 3 and Policy scale	Mix of Layer 2 and Layer 3 capabilities	Layer 3 and NAT scale

Customize table sizes for each function, based on the Place in Network

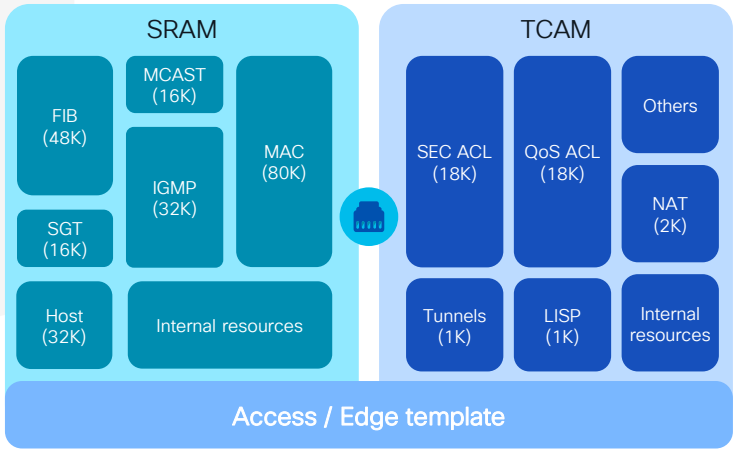
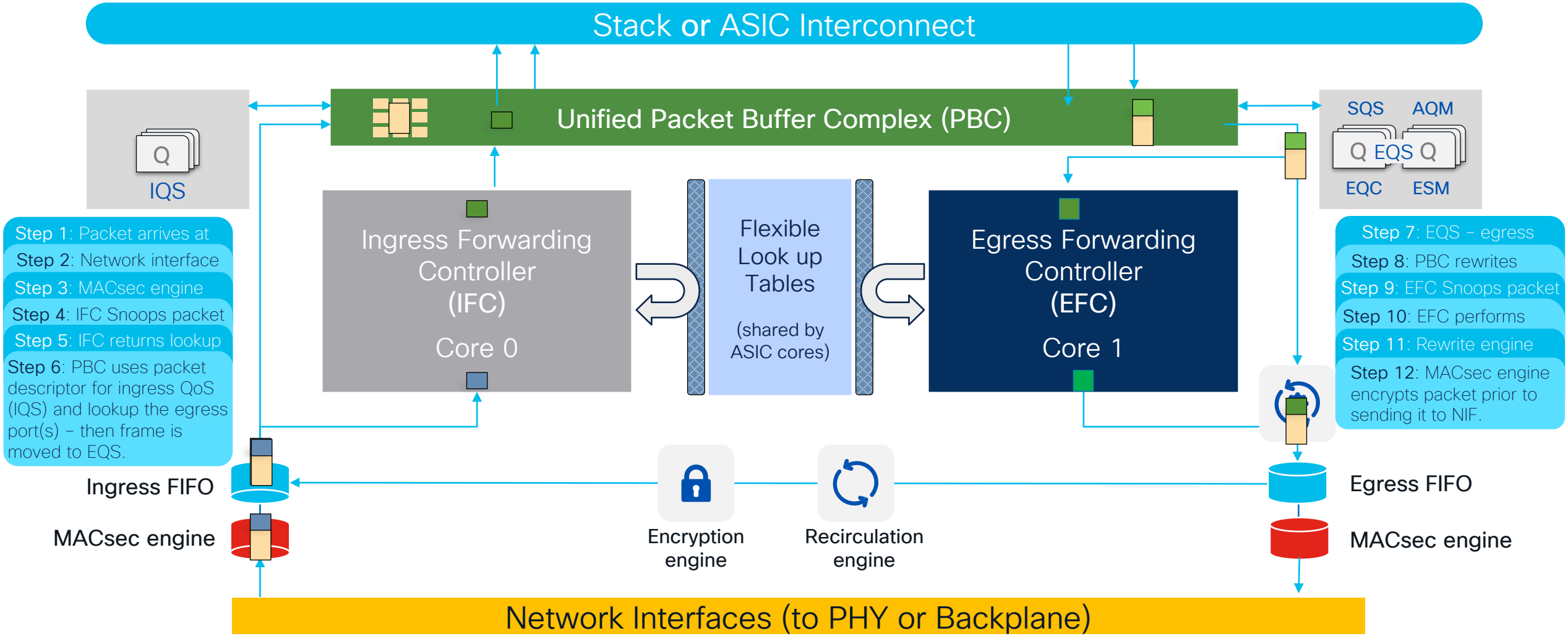


Table sizes can be tailored to support multiple templates

Cisco UADP – Packet Walks

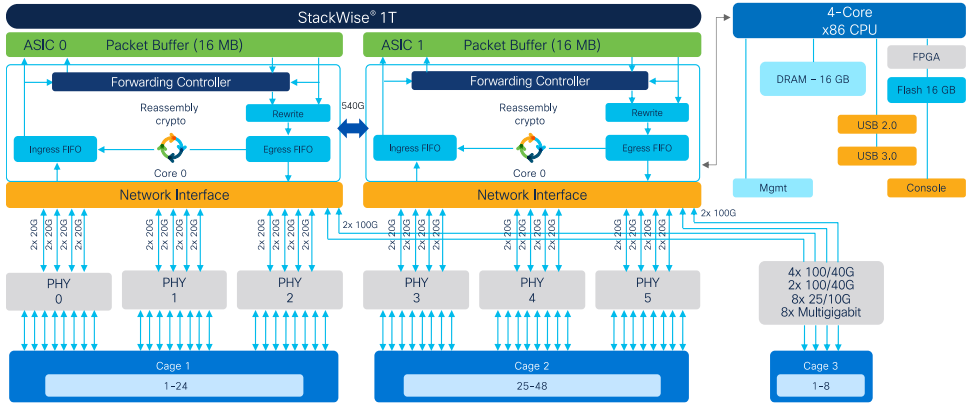
Generic Packet Walk – Unicast, Same ASIC



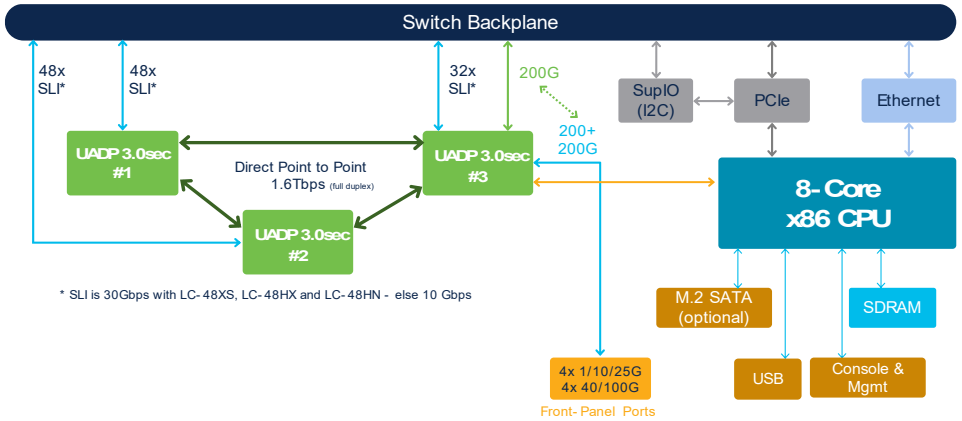
Cisco UADP on Cisco 9000 Switches

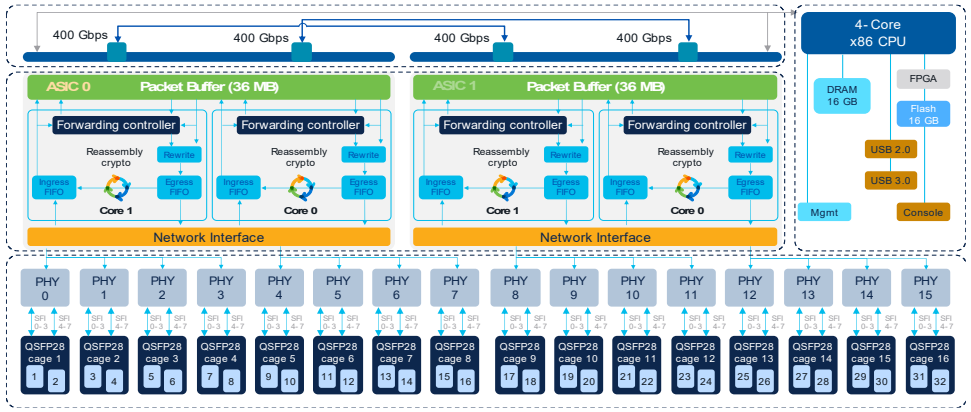
Common ASIC Architecture

C9300X-48HX

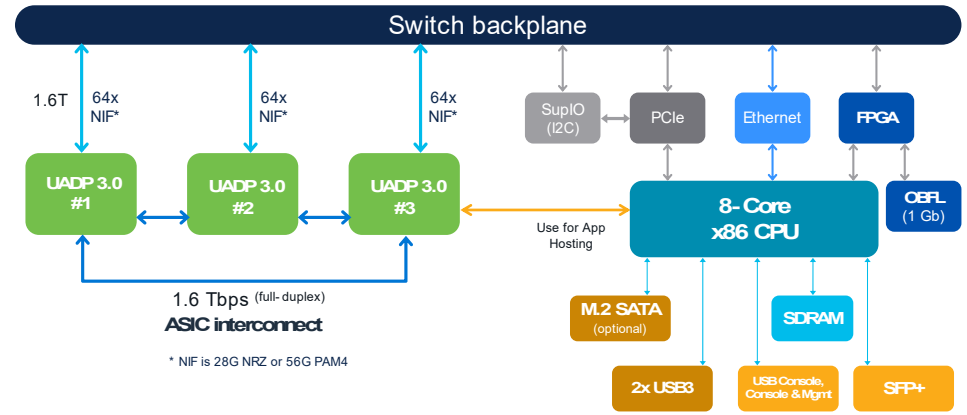


C9400X-SUP-2/XL



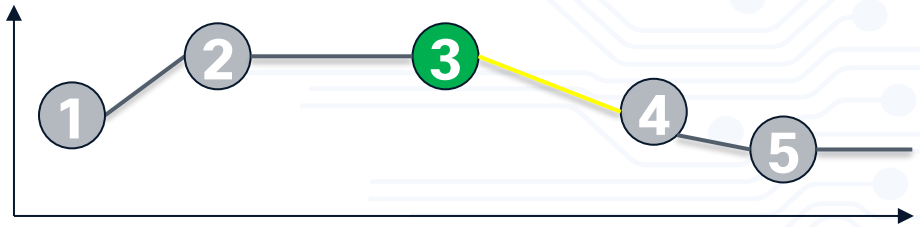


C9500-32C



C9600-SUP-1

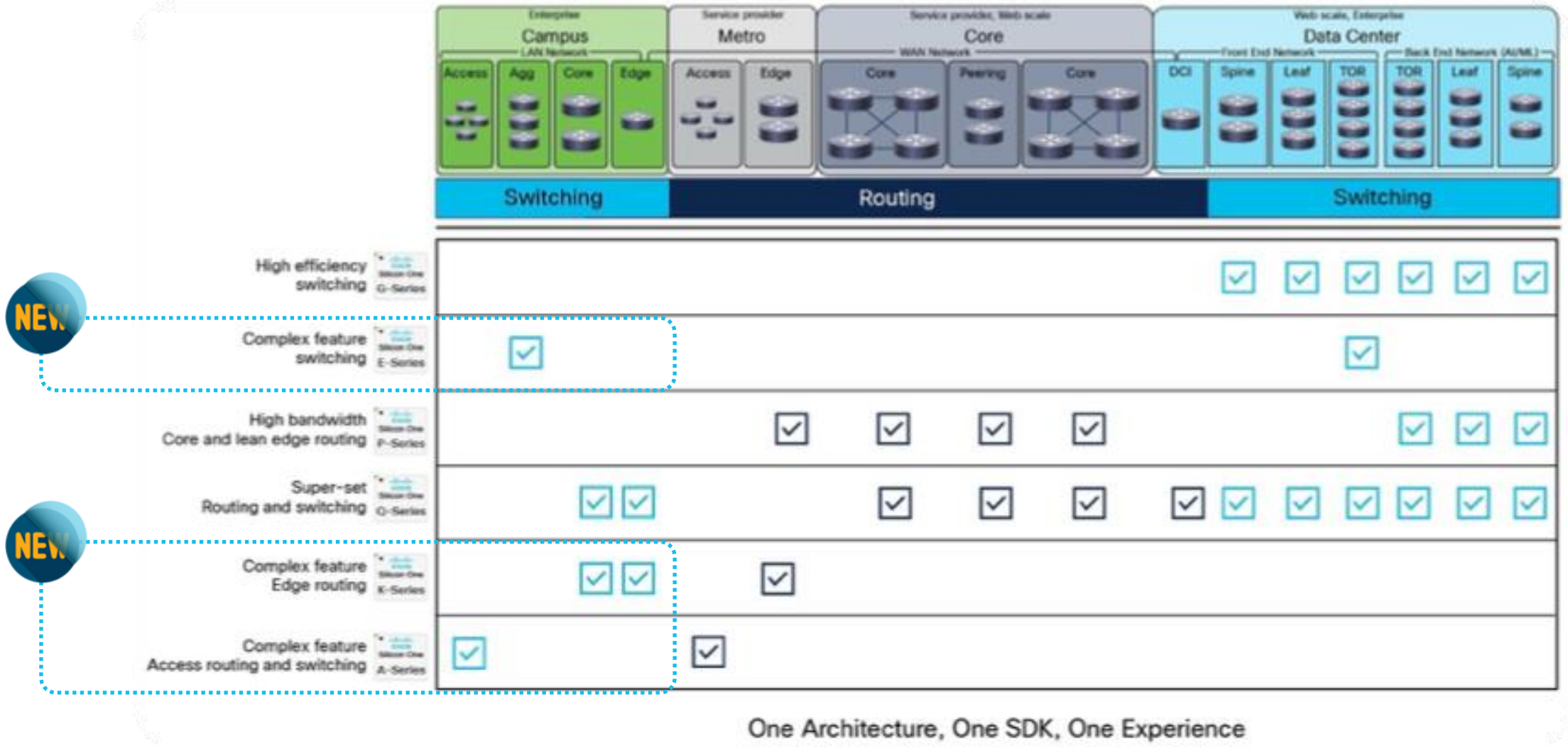
Cisco Silicon One™ for Enterprise Switching



Introducing Cisco Silicon One™

One Architecture - Multiple Devices

www.cisco.com/c/en/us/solutions/silicon-one.html



Multi-Slice ASIC Design

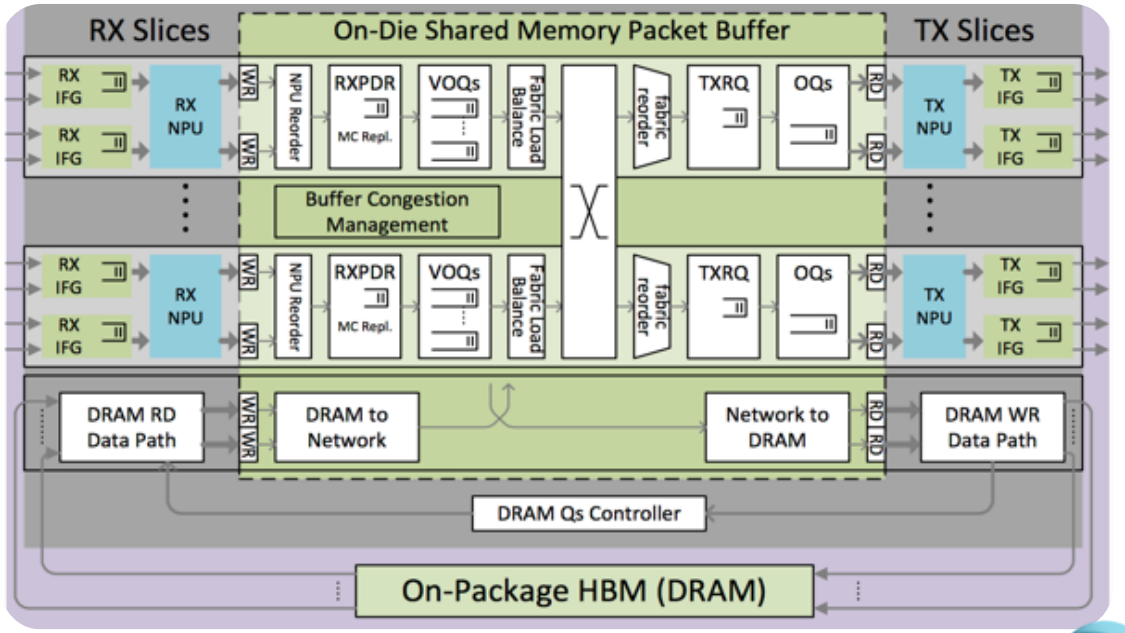
Combining multiple Pipelines in same ASIC

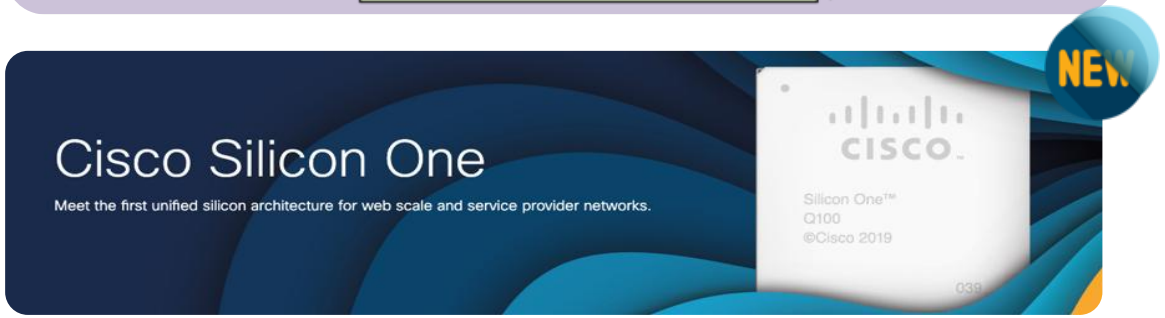
A new approach (like Multi-Core & Multi-ASIC) is to use **multiple full Network Processing Unit (NPU) pipelines** on a single ASIC package.

Each NPU pipeline (or 'Slice') **operates independently and connected via an integrated crossbar** "fabric", using an integrated Virtual Output Queue (VoQ) buffer architecture, to manage traffic between Slices.

Unlike Multi-Core (only multiplies "processing") **each Slice has dedicated RX/TX resources** for parsing, QoS, replication and other ASIC "forwarding" co ents.

TIP The new Cisco Silicon One Q100 & Q200 are examples of a Multi-Slice ASIC design





www.cisco.com/c/en/us/solutions/service-provider/innovation/silicon-one.html

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Cisco Silicon One™

One Architecture - Multiple Devices

www.cisco.com/c/en/us/solutions/collateral/silicon-one/silicon-one-wp.html

Q100

10.8 Tbps

16nm FinFET
6 Slice SOC
SMS + HBM*

Q200

12.8 Tbps

7nm FinFET
6 Slice SOC
SMS + HBM2*

NEW

A100

1.3 Tbps

16nm FinFET
1 Slice SOC
SMS + DDR4*

E100

6.4 Tbps

7nm FinFET
2 Slice SOC
SMS

K100

6.4 Tbps

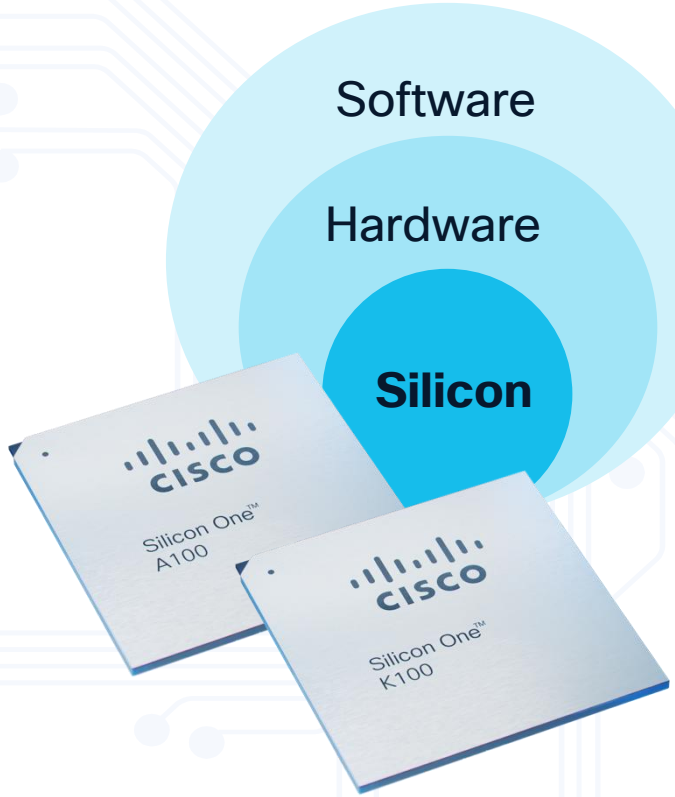
7nm FinFET
2 Slice SOC
SMS + HBM2E

- **Comprehensive routing, with switching efficiency**
- Onboard and expandable memories
- Flexible P4 NPL programmable packet processing
- **Multiple functions: system-on-chip, line-card or fabric**
- Multiple form factors: fixed or modular
- Multiple networks: Enterprise, Data Center and SP

10 Ways Cisco Silicon One Powers Campus Networking

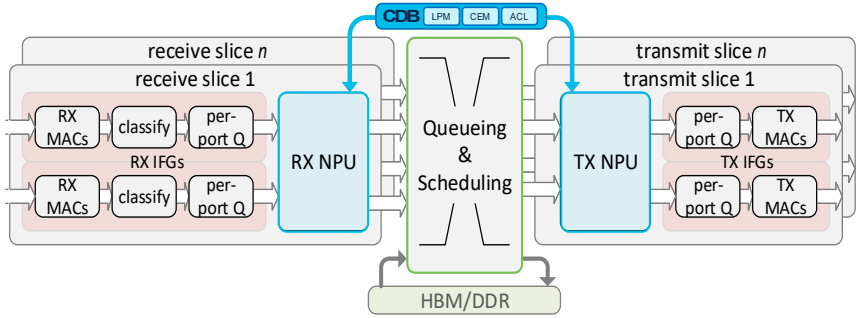
Innovative silicon features that deliver unmatched control, security, efficiency, and scalability

- Unified architecture
- Adaptable tables
- Shared memory
- Flexible Serdes
- Silicon One SDK
- Programable networking
- Intelligent load balancing
- Enhanced troubleshooting
- Hardware Root of Trust
- Native encryption and security



Catalyst 9000 with S1

Introducing the next-generation of Campus ASICs



Cisco C9350 Series

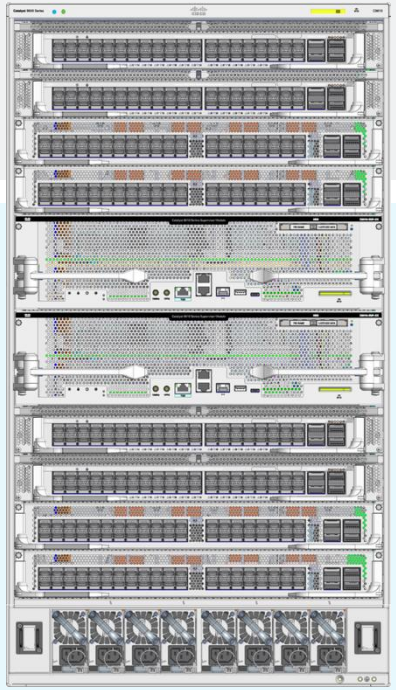
Powered by Cisco Silicon One **A100**

NEW

Cisco C9610-SUP-3 & 3XL

Powered by Cisco Silicon One **E100** & **K100**

NEW



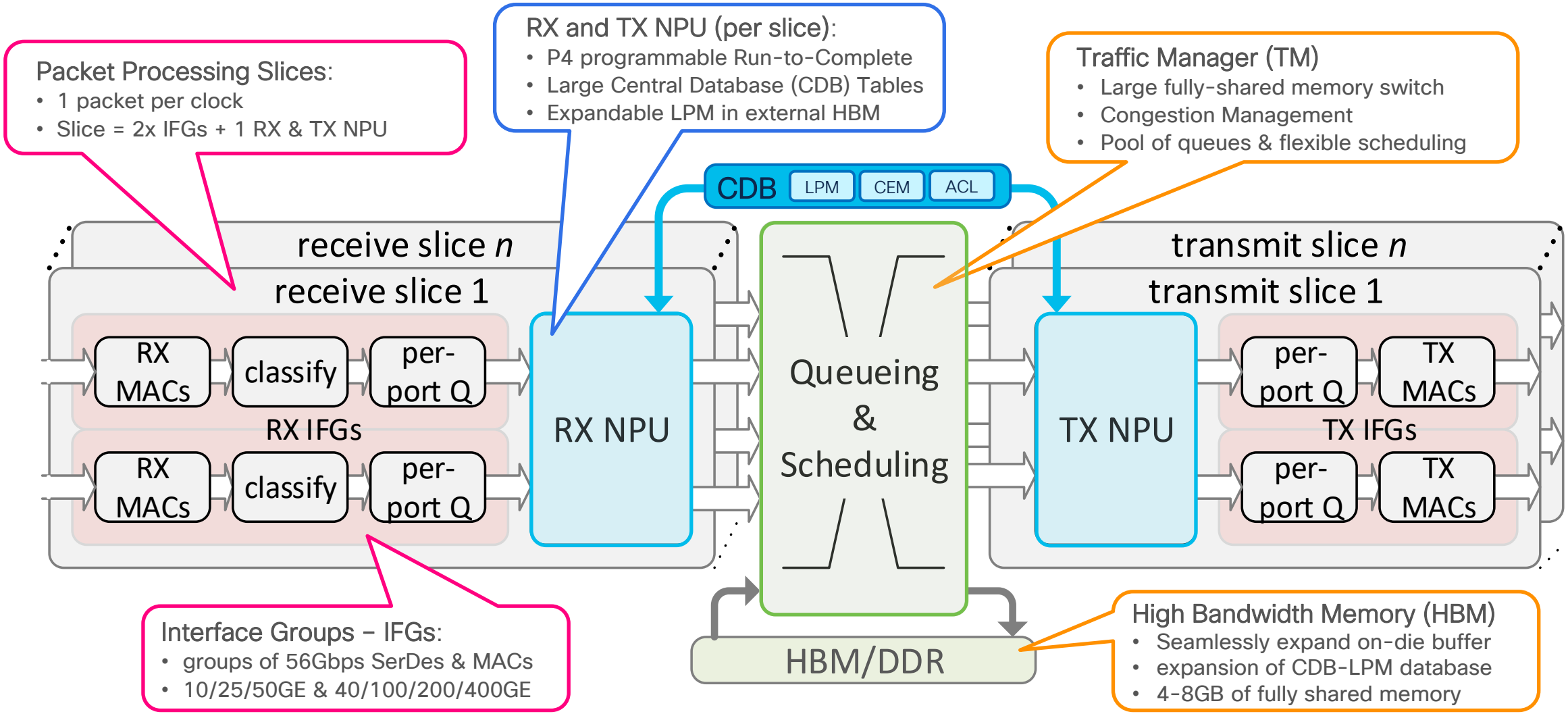
Catalyst 9500X & 9600X-SUP-2

Powered by Cisco Silicon One **Q200**

Cisco Silicon One™

ASIC Architecture & Block Diagram

up to **4 BILLION** times per second!



Cisco Silicon One™ – Central Databases

Onboard LPM, CEM & ACL memory

S1 CDB includes the **Central L2/L3 Forwarding** and **ACL** databases:

LPM – SRAM database for IP/mask routing implemented by Longest Prefix Match algorithm

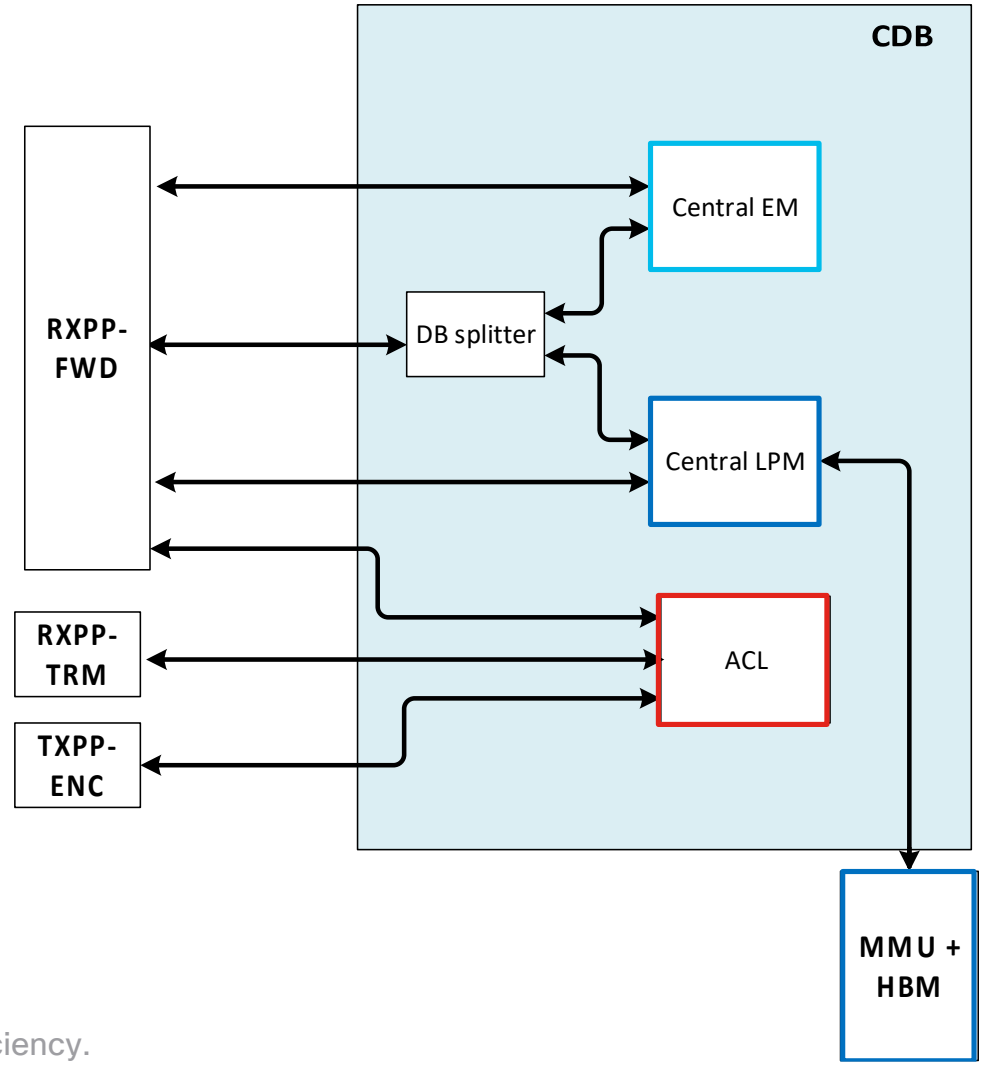
- Primarily used by IPv4 and IPv6 unicast routing
- LPM can be extended (from CDB) to HBM

CEM – SRAM database for MAC & Host (/48, /32 or /128), Multicast & Labels implemented by Exact Match algorithm

- For features using an exact match (every bit, no mask)
- CEM can be flexibly reallocated for different tables

ACL – TCAM classification database, contains Security, QoS and Services Access Control List entries

- For features that use (match criteria + action) policies
- Includes Security ACL (permit or deny)



* Exact scale depends on IP/mask distribution (contiguous vs. random) and hash efficiency.

Cisco S1 – Packet Processing Flow

System-wide Processing Context

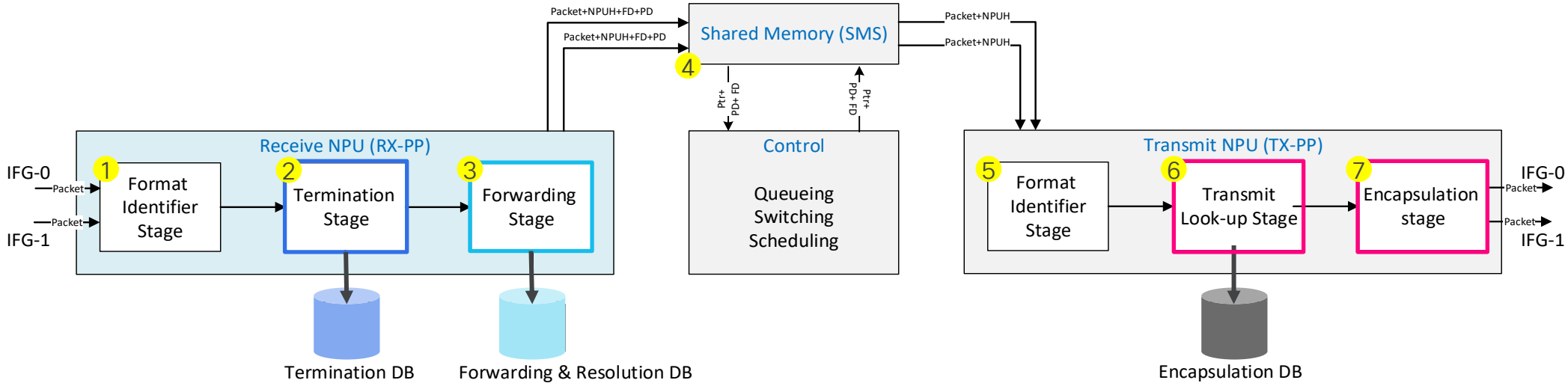
S1 NPU packet processing (pipeline) has **3 main stages**:

RX: 1. Termination and 2. Forwarding & Resolution and TX: 3. Transmit + Encapsulation

Termination — mainly used for **MAC & Tunnel termination** – to obtain the **L2 Logical Port (LP)** and **L2 Relay-ID** attributes, and/or (if MAC is not terminated) to obtain the **L3 LP** and **L3 Relay-ID** attributes.

Forwarding — **forwarding** (1st step) determines the **Destination Logical Port (DLP)** – then passes to **resolution** (2nd step) to resolve the destination logical port to the **Destination System Port (DSP)** & encap data.

Encapsulation — determines the final **transmit encapsulation** (based on data from the forwarding & resolution stage).



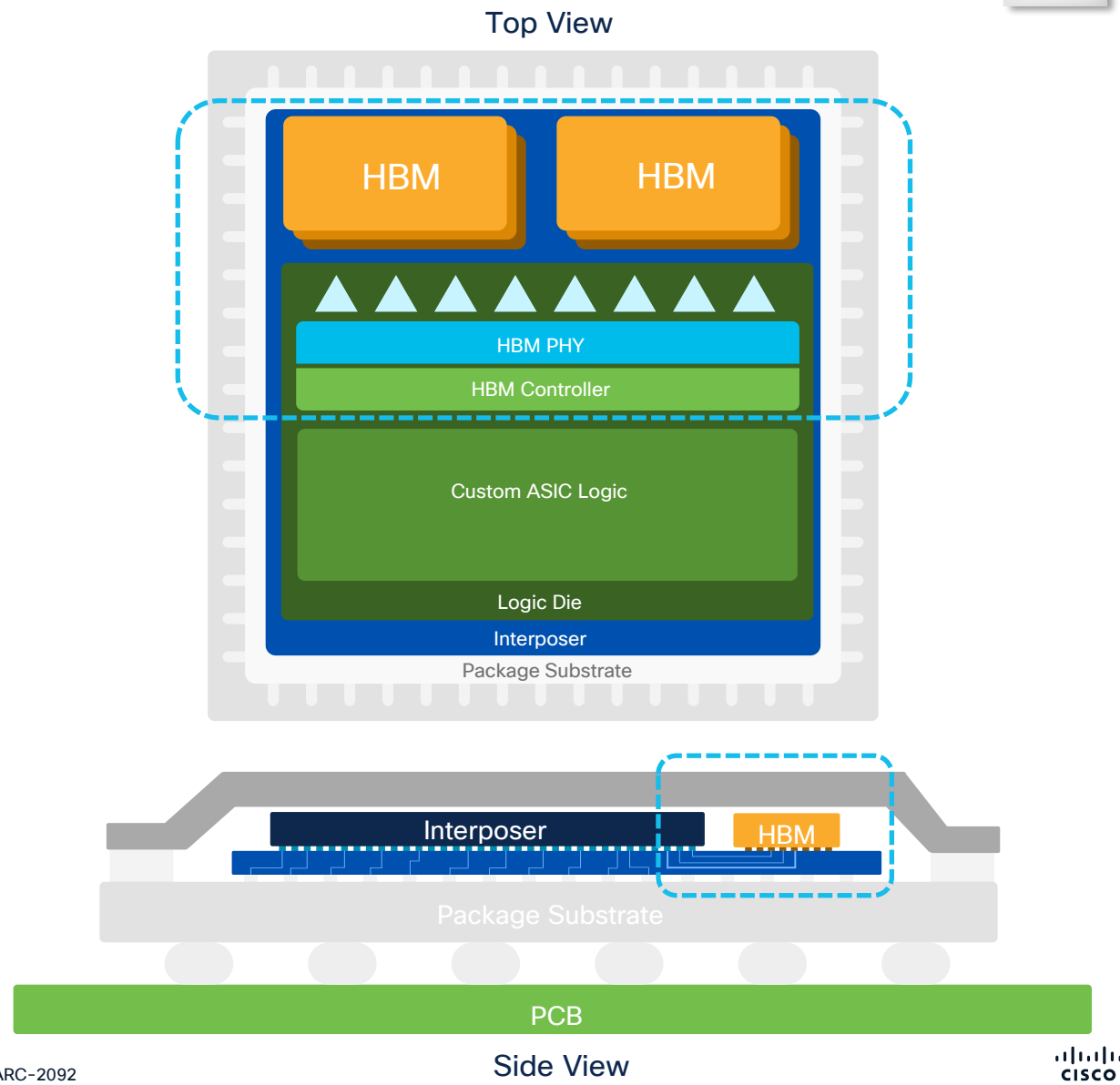
Cisco Silicon One – HBM

High Bandwidth Memory

en.wikipedia.org/wiki/High_Bandwidth_Memory

- **HBM achieves higher bandwidth*** using less power, in a substantially smaller form factor:
  - **2x stacks of HBM2E memory** = ~4.8 Tbps full duplex

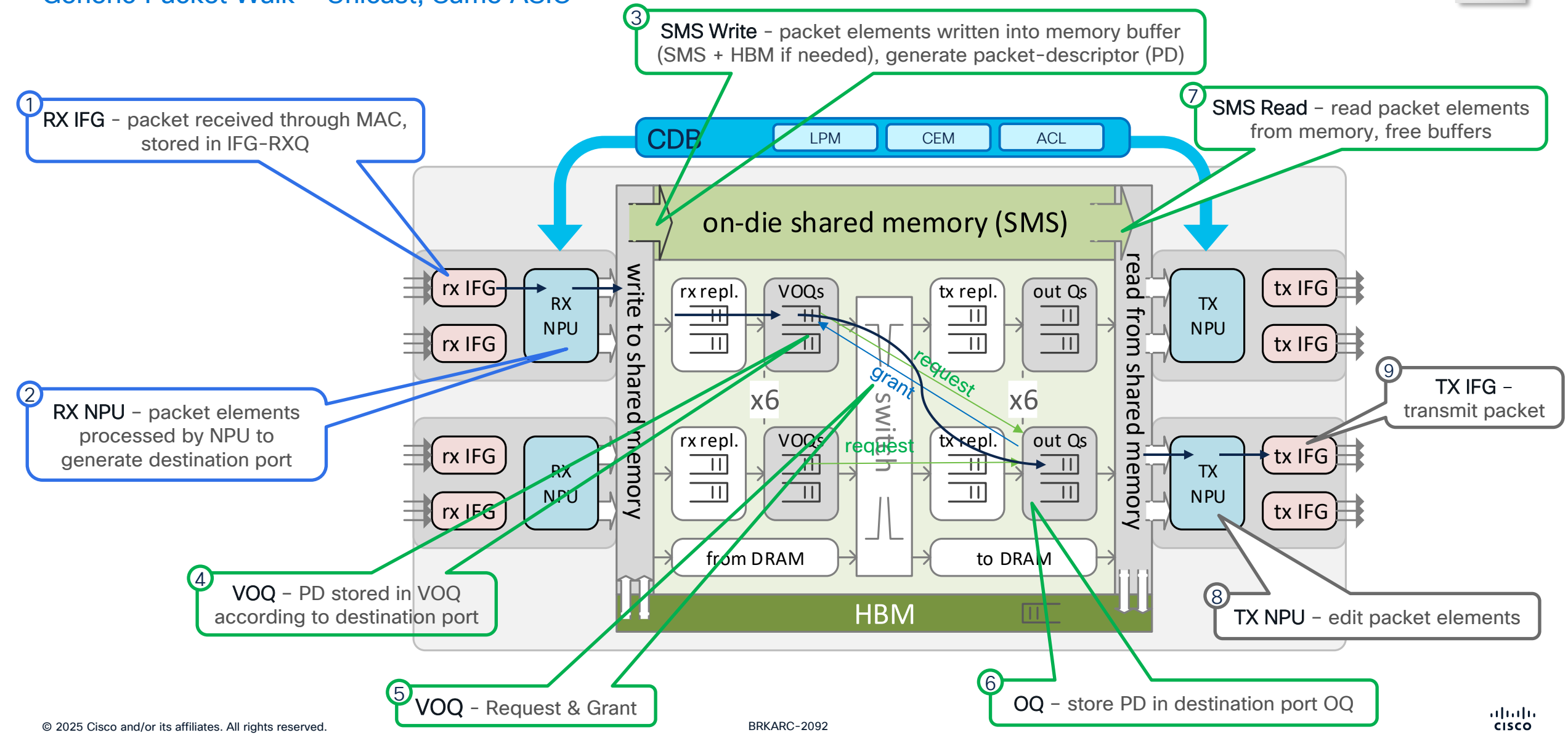
- **Augments local on-die memory**
  - buffer uses local (SMS) buffers until full
  - buffer uses HBM for bursts & congestion
- **Deep buffering + FIB expansion**
  - Interposer connects ASIC die to on-package HBM memory
  - local access at high-speed



*NOTE: higher bandwidth than DDR4 or GDDR5

Cisco Silicon One – Packet Walks

Generic Packet Walk – Unicast, Same ASIC



What's new in A100 & K100/E100?

Cisco Silicon One NPU 2.0 ASICs - Built for Enterprise Features

* Compared to S1 Q200 (NPU 1.0)

Shared innovative **S1 Architecture**

- Multi-Slice Run-To-Complete NPU
- Low Power with High-Performance
- P4-based NPL and Common SDK
- VOQ-based SMS and HBM/DDR
- Standalone, Module or Fabric mode

Newer **Longest Prefix Match (LPM)***

- High-scale IP/mask with HBM extension
- Improved efficiency with embedded Hash

Newer & larger **Exact Match (CEM)***

- High-scale MAC, ARP, Multicast, SGT, NAT, etc.
- More flexible for various 'exact match' features

New & larger **Policy Match (HCAM)***

- High-scale Algorithmic TCAM + Hash SRAM
- Robust support for ACL, QoS & FNF features
- Better Ingress and Egress policy support

NEW

Hardware **Flexible NetFlow***

- FNF records use HCAM (wide-entries)
- Support for AVC/NBAR and ETA/XDR

Hardware **Data Encryption***

- Embedded AES-GCM 256-Bit Crypto Engines
- Line-rate (LAN) MACsec
- Hardware WAN MACsec and IPsec

Hardware **Precision Time***

- Hardware PTP 1588, AVB, AES67 & G8275
- Support for IT/OT Frame Preemption

Advanced **QoS & Buffering***

- More VoQs, Policers and Shapers
- Enhanced WRED and HQoS

Flexible **Telemetry Counters***

- Millions of Programmable counters
- Configurable Feature allocation

Lower & Higher-Speed **Ports***

- 10/100/1000M and 2.5/5/10G mGig RJ45
- 1/10/25G/50G SFP and 40/100/400G QSFP

... and much more

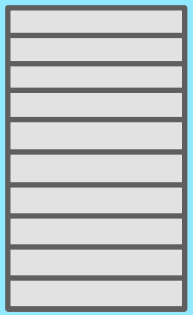
What is Cisco S1 HCAM?

Algorithmic Hash-based TCAM for High-Scale ACL & NetFlow

8K TCAM

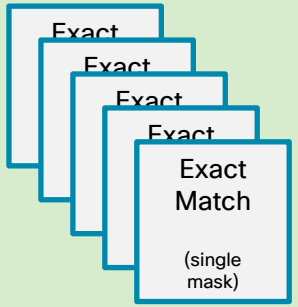
TCAM

- **Key based – variable mask**
- Supports flexible matching logic
- Complex & versatile searches
- Less-Dense (fewer bits in same area)
- Faster lookup speed
- Power & Heat intensive
- **Expensive to scale**



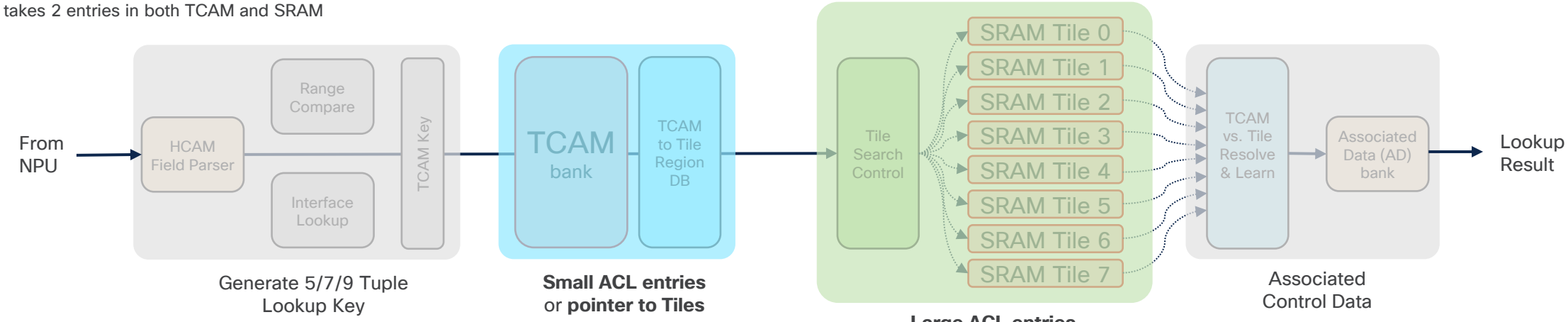
128K SRAM (8x Tiles of 16K)

SRAM
(Tiles)



- **Hash based – full mask**
- Simple, specific searches
- Rigid exact matching logic
- More-Dense (more bits in same area)
- Slightly slower speed
- Lower Power & Heat
- **Less costly to scale**

NOTE: IPv6 takes 2 entries in both TCAM and SRAM



Generate 5/7/9 Tuple Lookup Key

Small ACL entries or **pointer to Tiles**

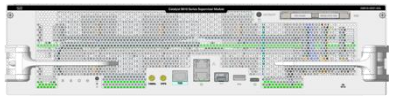
Large ACL entries or **NetFlow entries**

Associated Control Data

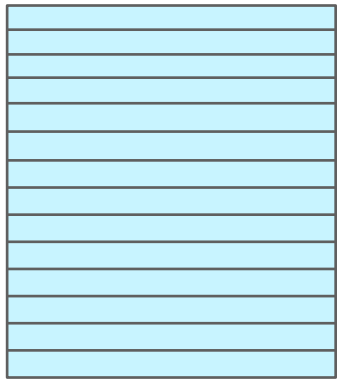
Flexible Scale with HCAM

ACL and FNF entry space sharing

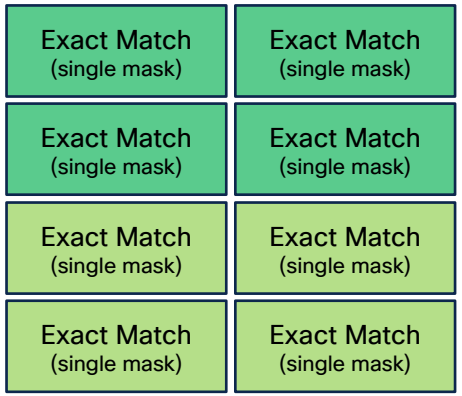
Algorithmic TCAM – the Best of Both Worlds



HCAM = TCAM + SRAM



TCAM

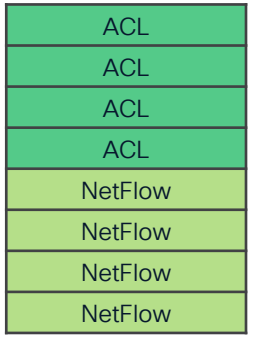


SRAM (8–32 tiles)

*Default SDM:
Half of each tile shared

Half reserved for ACL entries

Half reserved for NetFlow cache



C9350	C9610
• **16K** Ingress ACL Entries • **16K** Egress ACL Entries System (total)	• **32K** Ingress ACL Entries • **32K** Egress ACL Entries System (total)
• **32K** Ingress NetFlow • **32K** Egress NetFlow Per ASIC (x ASICs)	• **64K** Ingress NetFlow • **64K** Egress NetFlow Per ASIC (x ASICs)

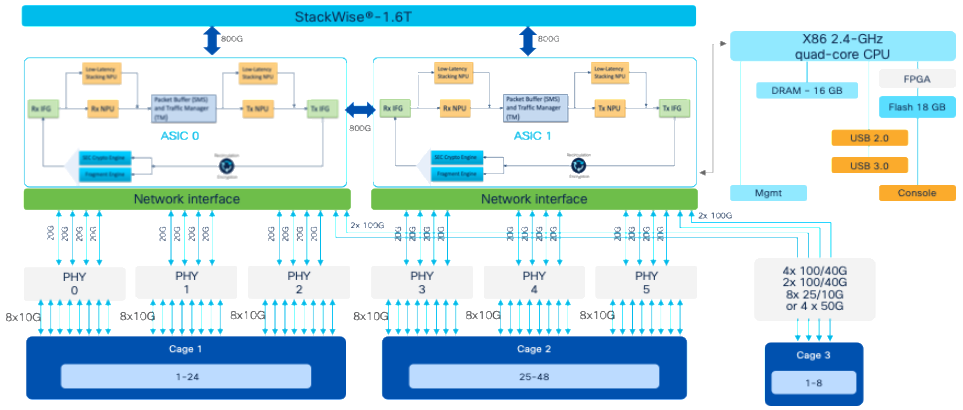
A100	K100
1x HCAM Shared by RX & TX	4x HCAM 2x RX 2x TX

* Based on Default SDM. ASIC capable of higher scale with Custom SDM (future software release)

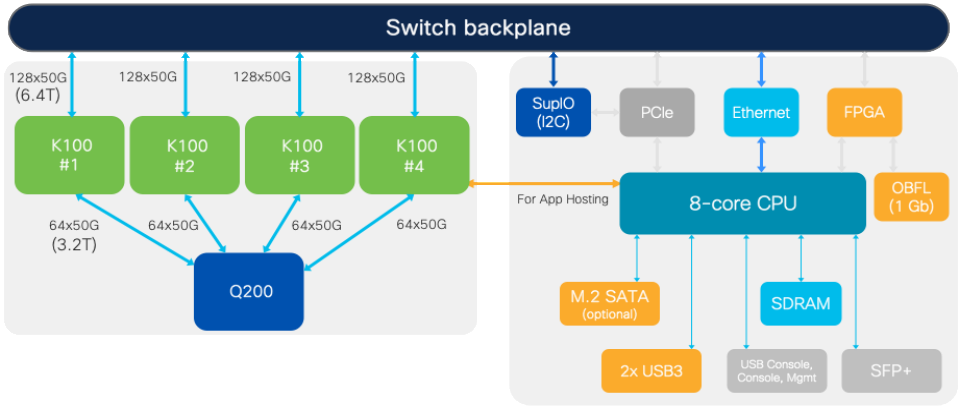
Cisco Silicon One on Cisco 9000 Switches

Common ASIC Architecture

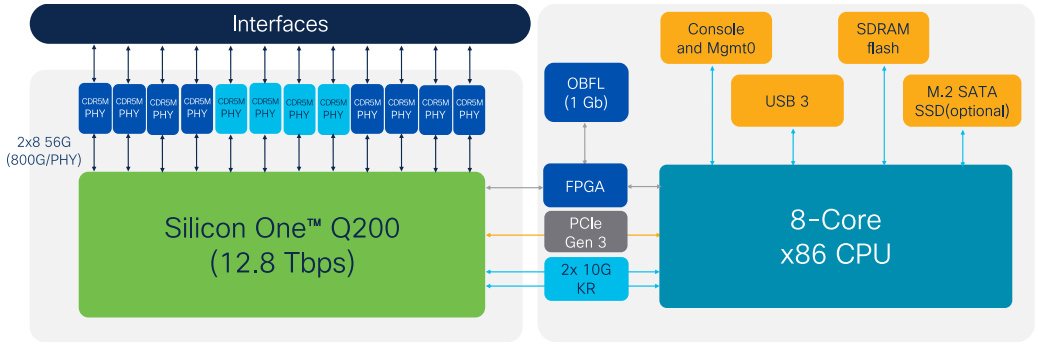
C9350-48HX & TX



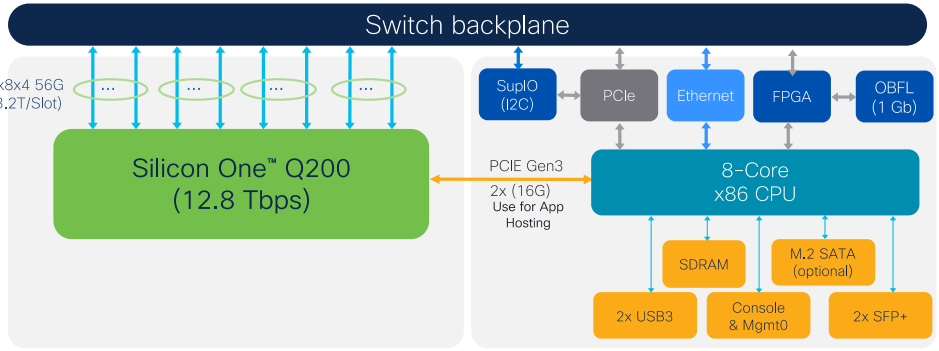
C9610-SUP-3/XL



C9500X-28C8D & 60L4D



C9600X-SUP-2



Cisco Silicon – ASIC Comparison

Contact PM/TME for latest status

● FCS+ HW & SW Committed

NOTICE: All scale numbers assume the 'Default' ASIC template

	S2 A100/L		UADP 2.0sec		UADP 2.0		UADP 1.1	
IP LPM Routes	**256K/128K**		**15K/7.5K**		**8K/4K**		**8K/4K**	
IP Host Routes	**96K/48K**		**32K/16K**		**32K/16K**		**32K/16K**	
MAC Address	**64K**		**32K**		**32K**		**32K**	
Multicast L2 groups	8K		8K		8K		4K	
Multicast L3 routes	8K/4K		8K/4K		8K/4K		4K/2K	
MPLS VPN Labels	32K		15K		7K		7K	
NAT/PAT	13K		5K		5K		--	
PBR	3K		3K		3K		1K	
SGT/OG ACL Labels	12K		5K		5K		3K	
Security ACL Entries	**16K**	**16K**	**4K**	**4K**	**2.5K**	**2.5K**	**1.5K**	**1.5K**
QoS ACL Entries	1K	1K	2K	2K	2K	2K	1K	1K
NetFlow Entries	**32K**	**32K**	**32K**	**32K**	**32K**	**32K**	**24K**	**24K**
Policers	4K		4K		4K		1K	
PVST Instances	1K		300		300		128	
VLANs	4K		1K		1K		1K	
VRFs/VPNs	256		256		256		64	

Cisco Silicon – ASIC Comparison

Contact PM/TME for latest status

● FCS+ HW & SW Committed

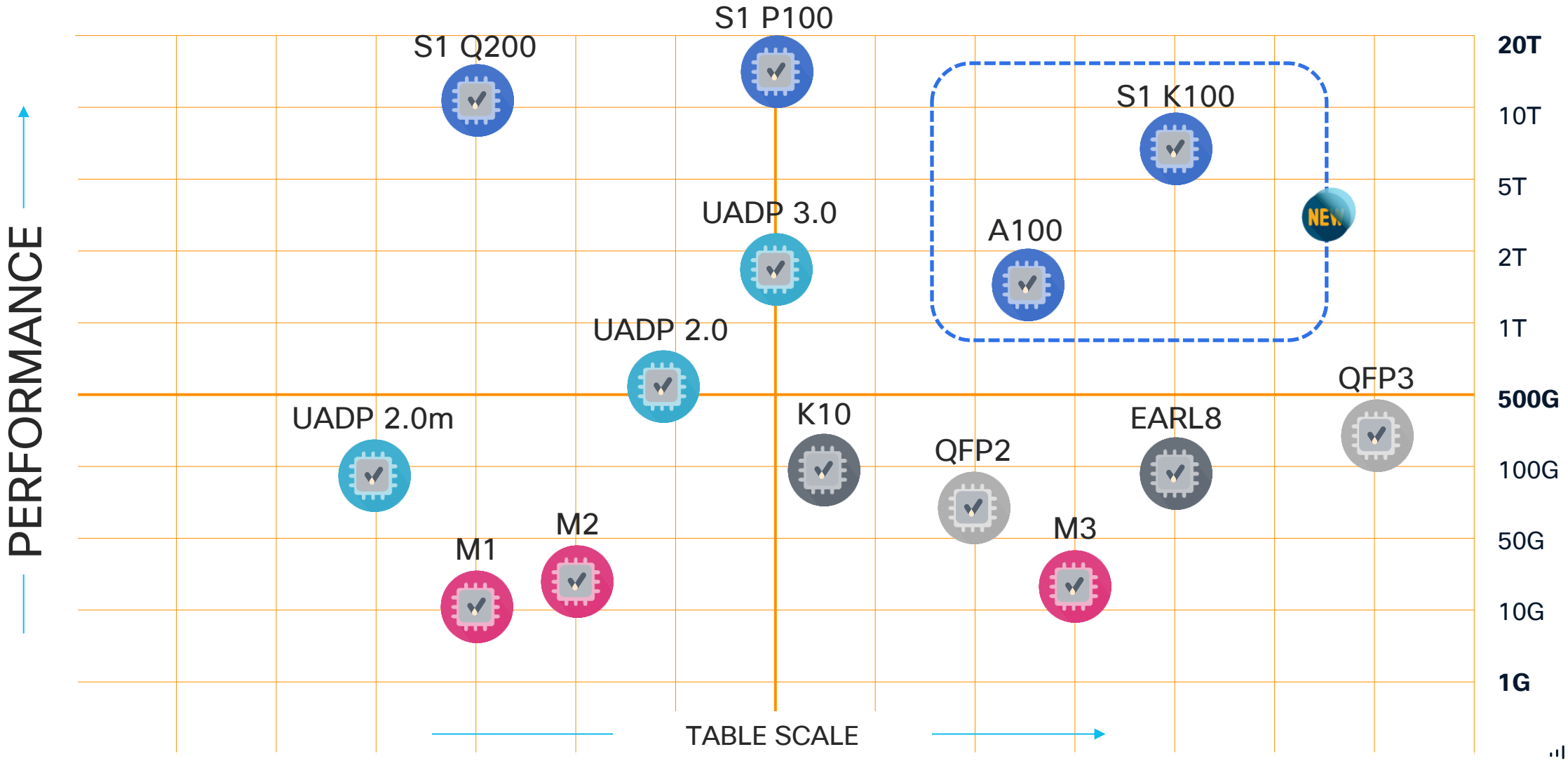
NOTICE: All scale numbers assume the 'Default' ASIC template

	S1 E100		S1 K100		S1 Q200		UADP 3	
IP LPM Routes	**1M / 512K**		**2M / 1M**		**1.5M / 600K**		**212K**	
IP Host Routes	**128K**		**128K**		**128K**		**32K**	
MAC Address	**128K**		**128K**		**128K**		**32K**	
Multicast L2 groups	8K		16K		16K		16K	
Multicast L3 routes	32K		48K		32K		32K	
MPLS VPN Labels	64K		64K		64K		32K	
● NAT/PAT	128K		256K		---		15K	
PBR	4K		16K		16K		3K	
SGT/OG ACL Labels	24K		24K		24K		24K	
Security ACL Entries	**21K**	**21K**	**38K**	**38K**	**8K**	**1K**	**12K**	**15K**
QoS ACL Entries	1K	512	1K	512	1K	512	8K	8K
Flexible NetFlow Entries	**64K** (64K x2)	**64K** (64K x2)	**128K** (64K x2)	**128K** (64K x2)	-- **2M** (SW @ 10Mpps)		**96K** (32K x3)	**96K** (32K x3)
Policers	8K		16K		8K		4K	
PVST Instances	4K		4K		4K		1K	
VLANs	4K		4K		4K		4K	
VRFs/VPNs	4K		4K		4K		4K	

cisco

Cisco Forwarding ASICs

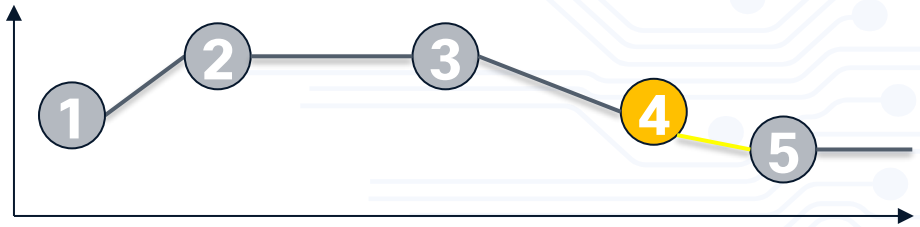
Processor Performance vs. Features Landscape



* details are approximate

Cisco 9000 Series Smart Switches

Extending Enterprise Switching



Catalyst 9200/CX, 9300/X & 9400/X

BRKARC-2098

Cisco 9000 Series Switching Family – **Access**

Manish Sharma – Technical Marketing, Cisco

This session will cover the platform overview of Cisco Catalyst 9000 Series access switches.

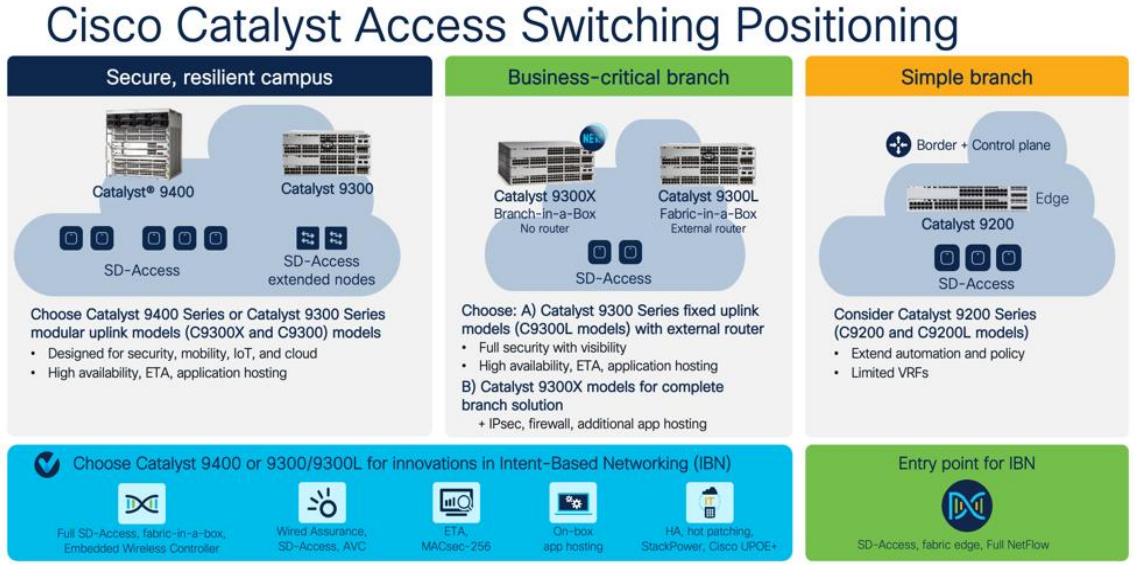
It will share the details of the Catalyst 9000 product portfolio, which will include new additions in **fixed and modular access series** – **Catalyst 9200, Catalyst 9300X and Catalyst 9400X**.

The session will talk about the component at the heart of these switches, which is the ASIC. It will also cover common attributes, technologies, and features in the Catalyst 9000 Series switches.

CiscoLive US 2025

Introducing **Cisco C9350 Series Smart Switches**

www.ciscolive.com/c/dam/r/ciscolive/global-event/docs/2025/pdf/BRKARC-2098.pdf



Introducing C9350 Series

3rd Generation Fixed Access/Aggregation – Stacking up Industry Firsts

NEW

MultiGigabit Downlinks

C9350-48HX

C9350-48TX

10/100/1000M Downlinks

C9350-48U

C9350-24U

C9350-48P

C9350-24P

C9350-48T

C9350-24T

Gen 3 Chassis

1.5 Tbps
System Capacity

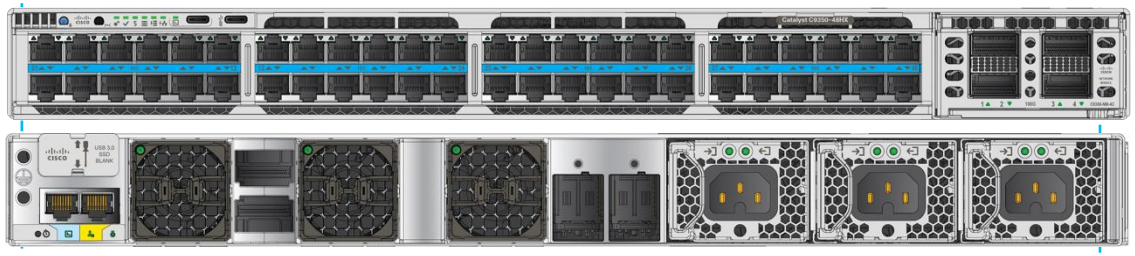
48x MGig and
48x UPOE+

16GB DDR4
memory

4 core X86 CPU
@2.0 Ghz

1.6 Tbps
NG Stacking

8-12* **Member**
NG Stacking



3x Modular
Fan Units

Front-to-Back (default) Back-to-Front

Reversible Airflow

New Stacking
& StackPower+

50CM-1M-3M

30CM-150CM

3x Modular
Power Supplies

1600W AC PS

850W AC 500W AC

Titanium Rated Platinum Rated

(1600W @220 & 1200W @110V)

Powered by Silicon One

Enterprise Focused
A100/L

256K **IPv4 / 128K IPv6**

64K MAC **64K ARP**

32K ACL **32K FNF**

Modular Uplinks

NM-4C

NM-2C

NM-8Y

*Hardware Capable

NOTE: Now with optional RFID for all components. (Choose on ordering)

Cisco 9500/X, 9600/X

BRKARC-2099

Cisco 9000 Series Switching Family – **Core & Distribution**

Kenny Lei - Leader Technical Marketing, Cisco

This session will cover the platform overview of Catalyst 9000 Series core and distribution switches.

It will share the details of the Catalyst 9000 Series product portfolio, which will include new additions in **fixed and modular core and distribution switching series - Catalyst 9500/X and Catalyst 9600/X**.

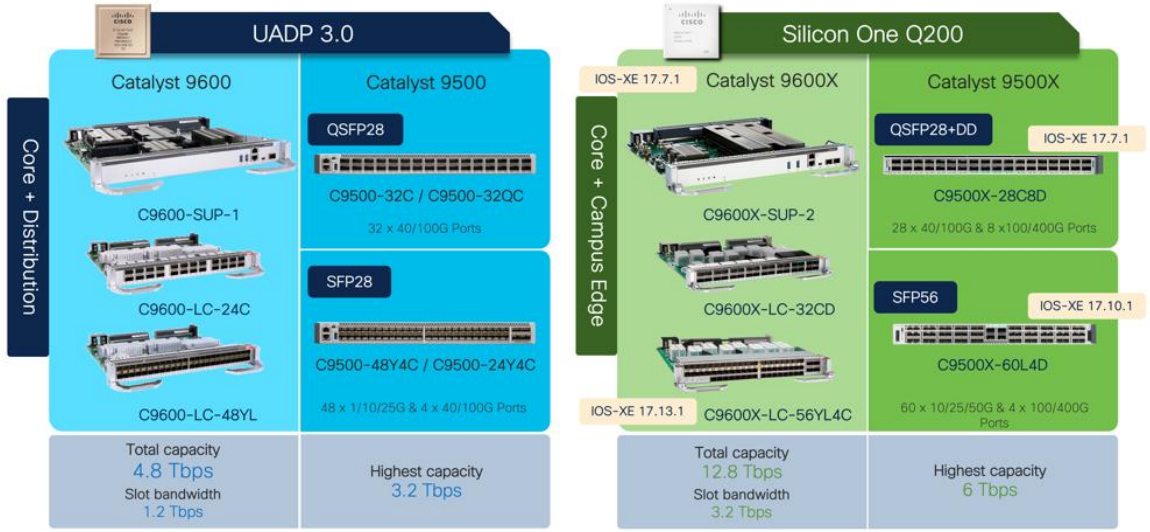
The session will discuss the component at the heart of these switches, which is the ASIC, and it will also cover common attributes, technologies, and features in Catalyst 9000 switches.

Cisco Live! San Diego, CA | June 8-12, 2025

CiscoLive US 2025

Introducing **Cisco C9610 Series Smart Switches**

www.ciscolive.com/c/dam/r/ciscolive/global-event/docs/2025/pdf/BRKARC-2099.pdf



Also check out BRKARC-2668

Introducing C9610 Series

3rd Generation Modular Core – with maximum port density

Gen 3 Supervisors

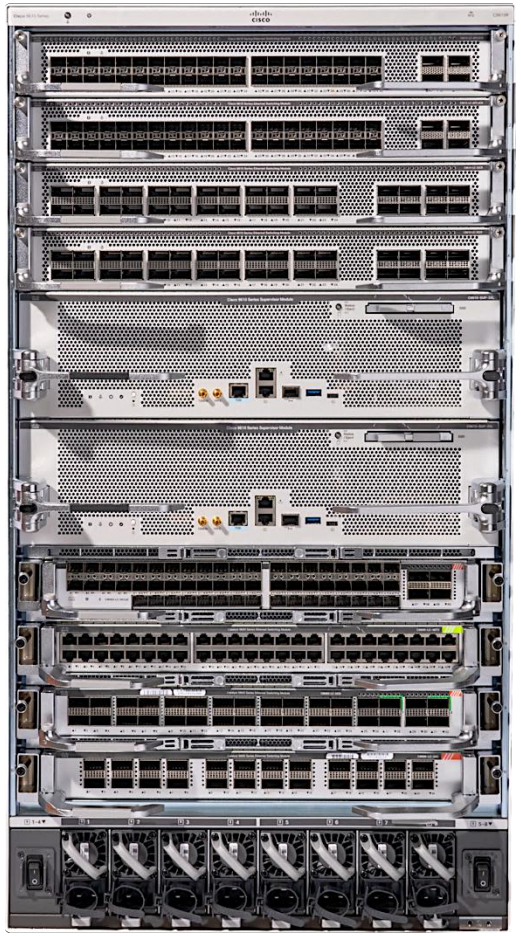
C9610-SUP-3/3XL

Enterprise Focus
K100/E100

- 2M **IPv4 / 1M IPv6**
- **3.2 Tbps** per slot
- **512K MAC & ARP***
- **32GB** DDR4 memory
- **256K ACL & FNF***
- **8 core** X86 CPU @2.0 Ghz

*Hardware Capable

Gen 3 Chassis



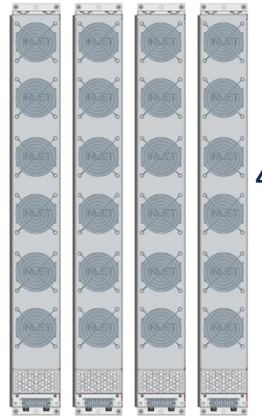
C9610R

- **51.2 Tbps** System Bandwidth
- **8-line card slots** (1.25 RU)
- **2 supervisor slots** (2.5 RU)
- **4 fan trays** serviceable in rear
- **Blue Beacons** (Chassis, Fans, Sups, & Line-Cards)
- **8 power supplies** AC/DC

Gen 3 Line cards

C9610-LC-40YL4CD

C9610-LC-32CD

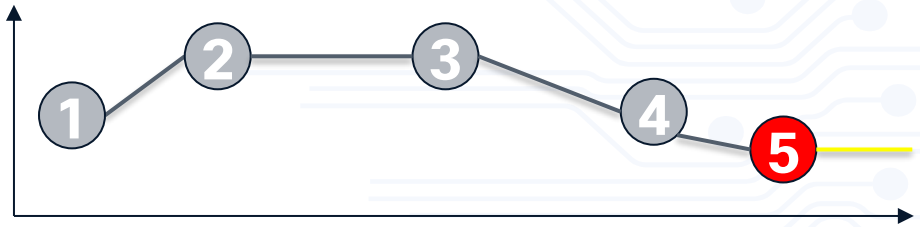


4x FAN Trays
with Front to Back Airflow

NOTE: Now with optional RFID for all components. (Choose on ordering)

Glimpse into the Future

ASIC Innovations for Enterprise Switching

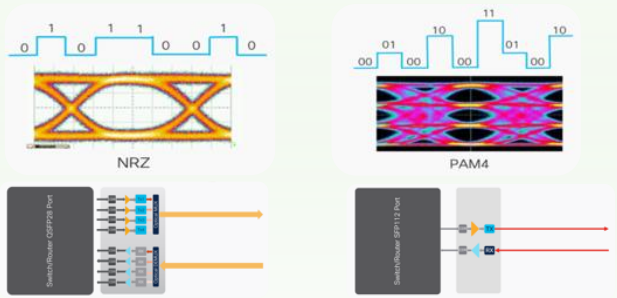


Where are things going?

Speeds and Feeds

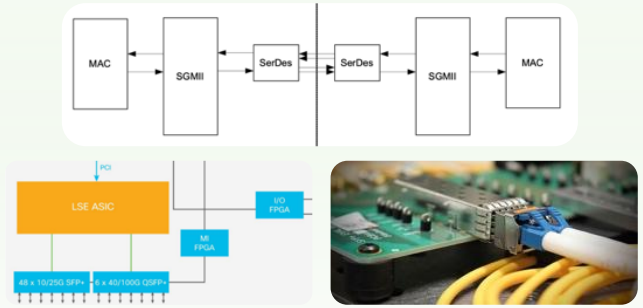
More details in PPT Notes

Single Lambda



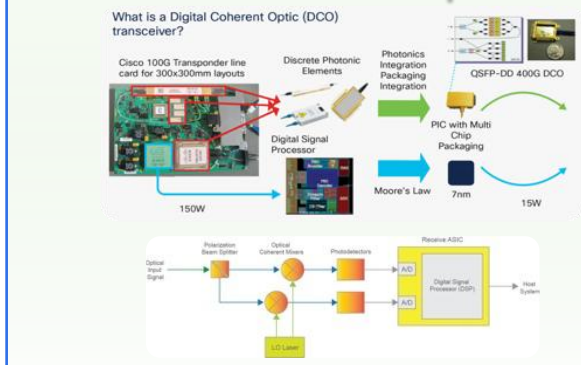
Uses a **single 112G PAM4** signal
vs. 4 x 28G NRZ signals

Direct-Drive (PHYLESS)



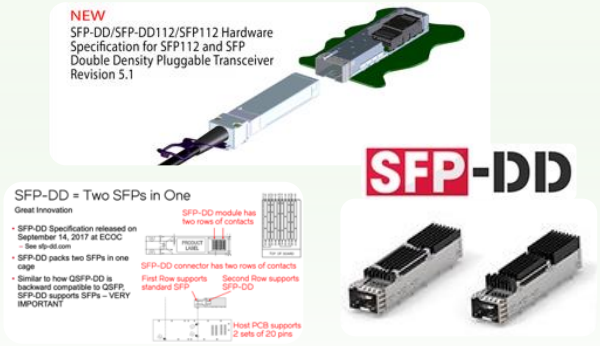
Transceiver **uses SFI/SGMII** to connect
directly to the **ASIC SerDes** (no PHY)

Coherent Optics



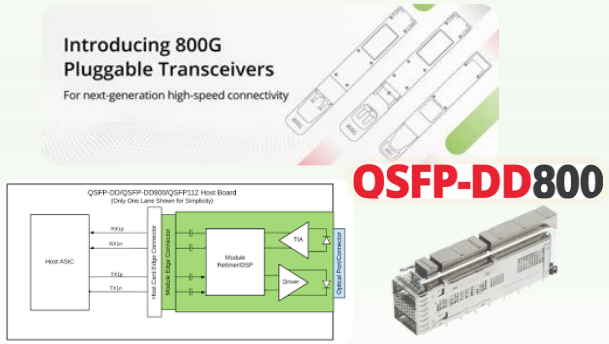
Uses **phase of optical signal** vs. power level

25/50G → 100G SFP



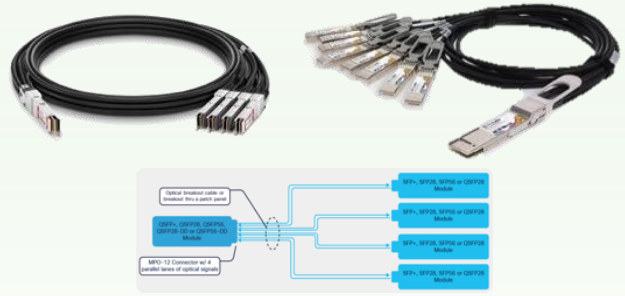
SFP-DD(112): 100Gbit/s using **PAM4**

100/400G → 800G QSFP



QSFP-DD(112): 800Gbit/s using **PAM4**

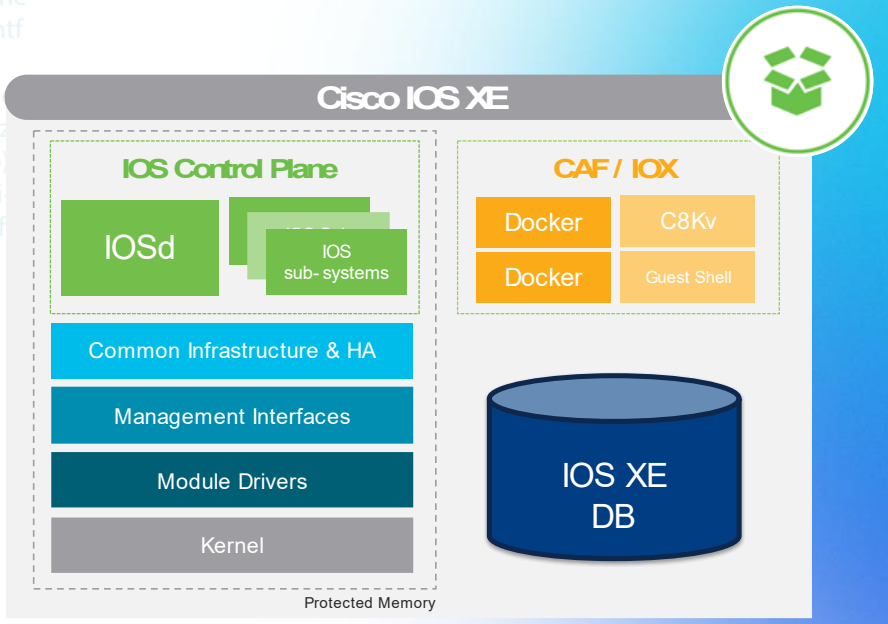
4x100G & 8x50G Breakout



QSFP-DD (400G) can be split into
4 x 100G QSFP28 or **8 x 50G SFP56**

Cisco IOS XE Software Architecture & Innovations

Cisco C9000 Series



Agenda

01 Brief History of IOS XE

02 Basic IOS XE Components

03 IOS XE Technologies

04 C9K IOS XE upto 17.15.1

05 C9K IOS XE after 17.18.1

06 Summary & Closing

Catalyst 9000 Series – Common Building Blocks

Multi-Core x86 CPU

Application Hosting
Secure Containers

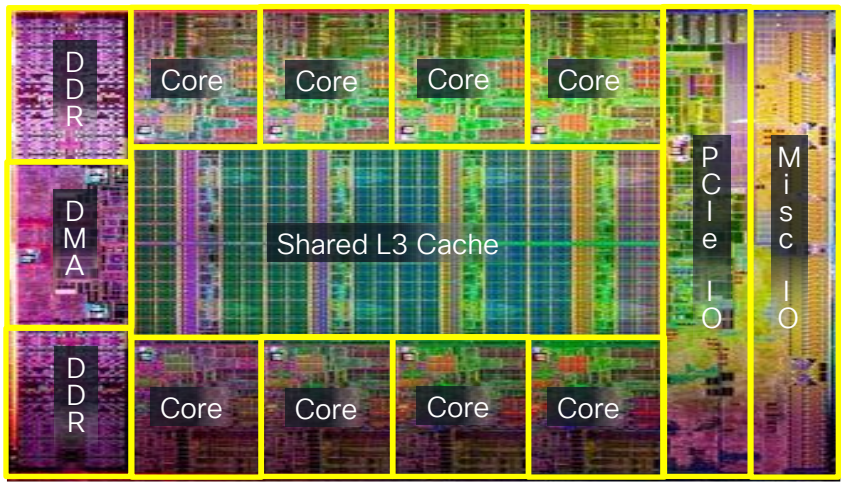
Cisco IOS XE®

Model-Driven APIs
Modular Patching

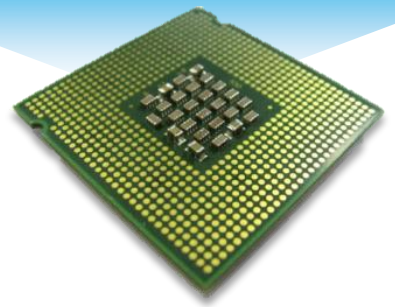
Cisco UADP & Silicon One™

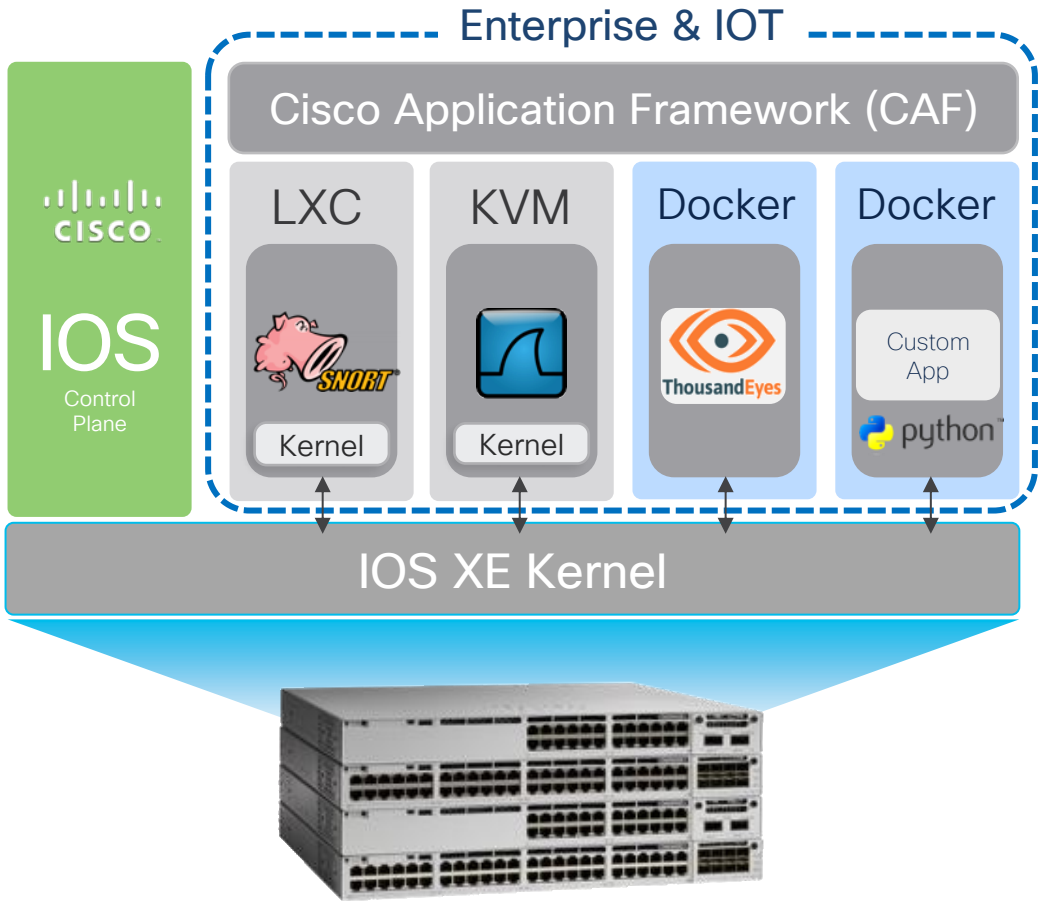
Programmable Pipeline
Flexible Tables

Multi-Core CPU – Built for App Hosting



x86 CPU

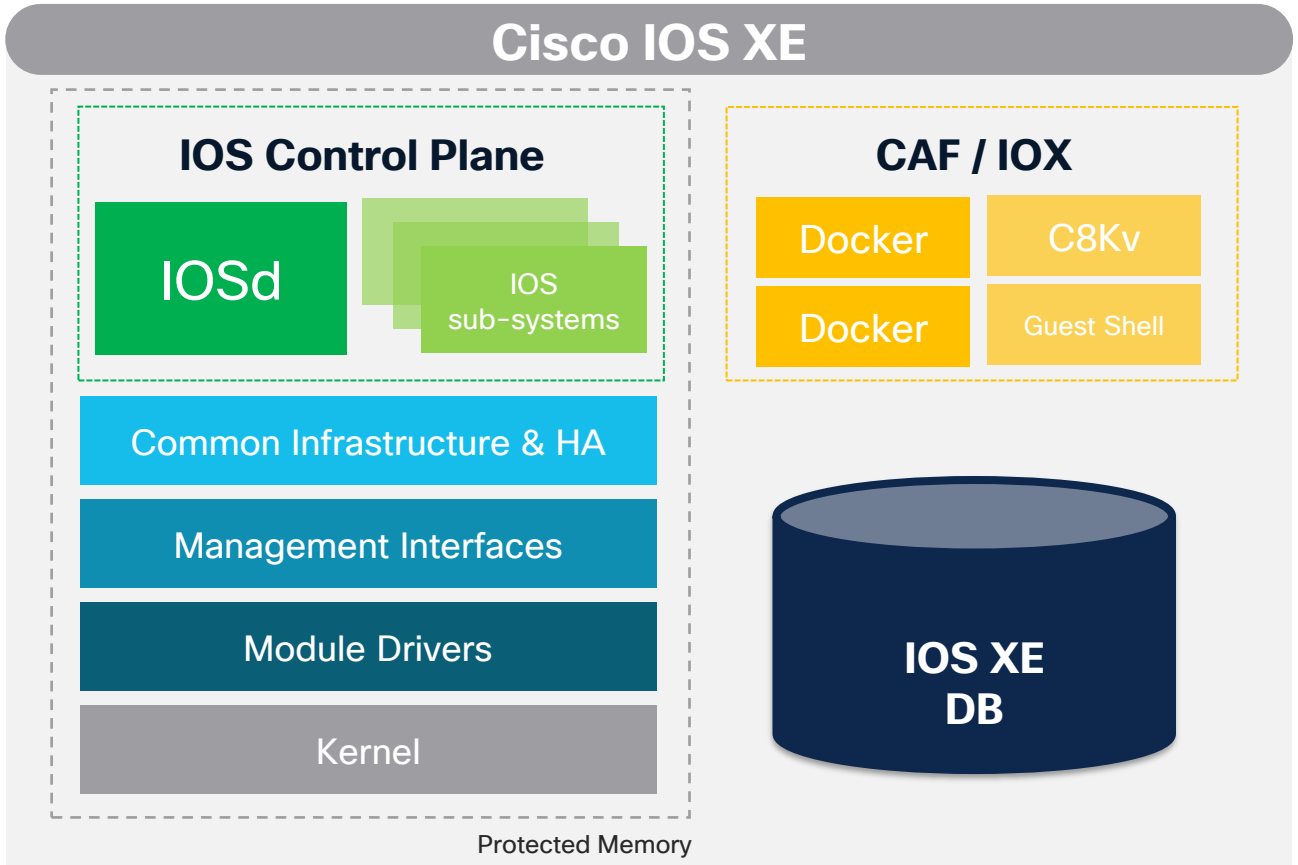




x86 CPU enables hosting NFV devices, Containers and 3rd-party Apps

* Catalyst 9200 Series uses an embedded ARMv8 CPU

Cisco IOS XE – A Modern Operating System



Cisco IOS subsystems
Resiliency and High Availability

Cisco IOS XE database
Programmability and Open models

IOX + Docker containers
Cisco and 3rd-party App hosting

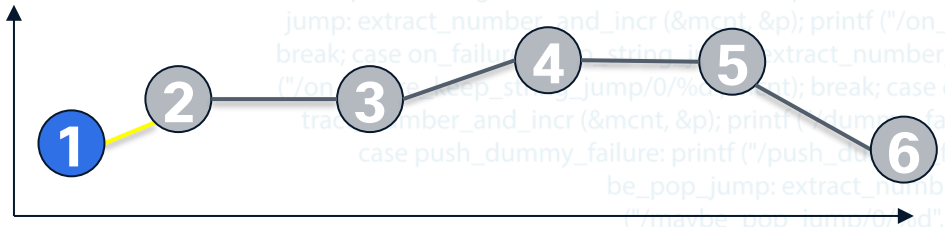
Open, Model Driven & Secure Operating System – Over 3000 Features

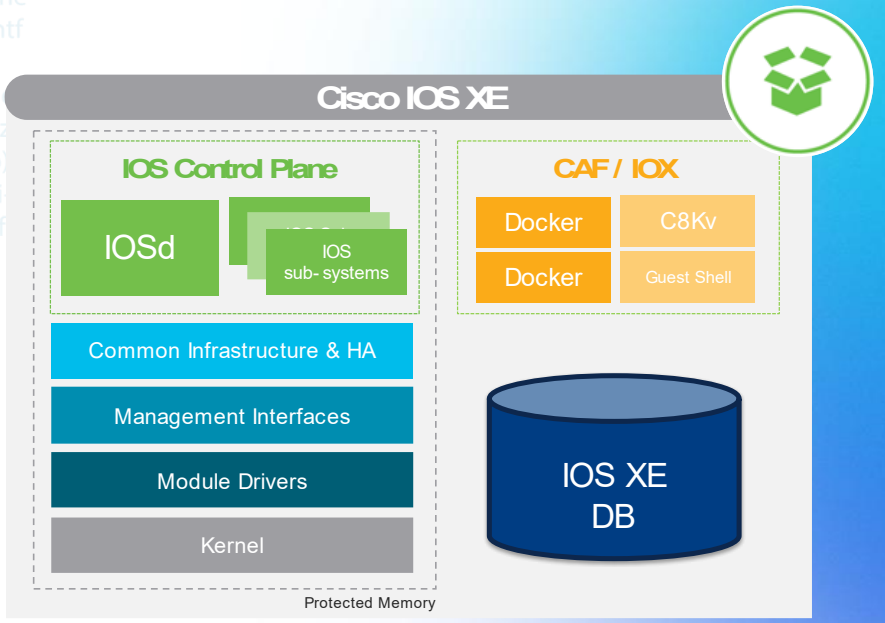
History of Cisco IOS®

Cisco IOS evolved into IOS XE

Nova IOS XE (Catalyst 3K)

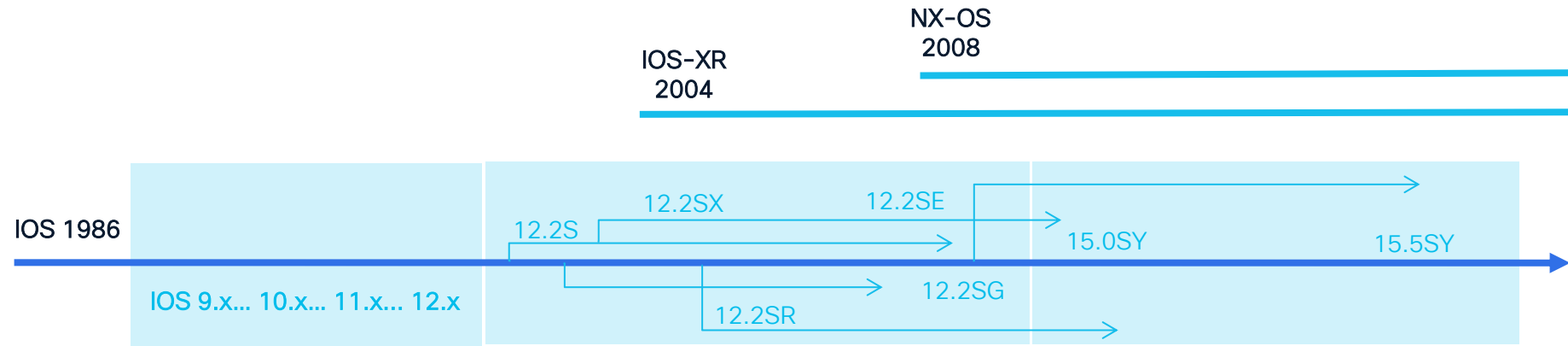
Polaris IOS XE (Catalyst 9K)



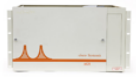


Brief History of Cisco IOS

NOTE: Timeline is just an approximation



1984	1986	1993	2000	2007	2009	2010	2015	2017
Cisco was born	Operating System 6.0	IOS 9.x – 11.x	IOS 12.x S Release	IOS XE BinOS 3.x	IOS 15.x M&T Release	IOS XE NOVA 3.x	IOS XE Polaris 16.1.1	Open IOS XE Polaris 16.5.1
	Cisco Ships First AGS Router	LAN Switching, WAN Switching	Cat6500, 7600 Series	ASR1000 Series	Cat6800 Series	Cat4500 Series Cat3850	Cat3850-XS, ASR-X, ISR	Catalyst 9000 Series

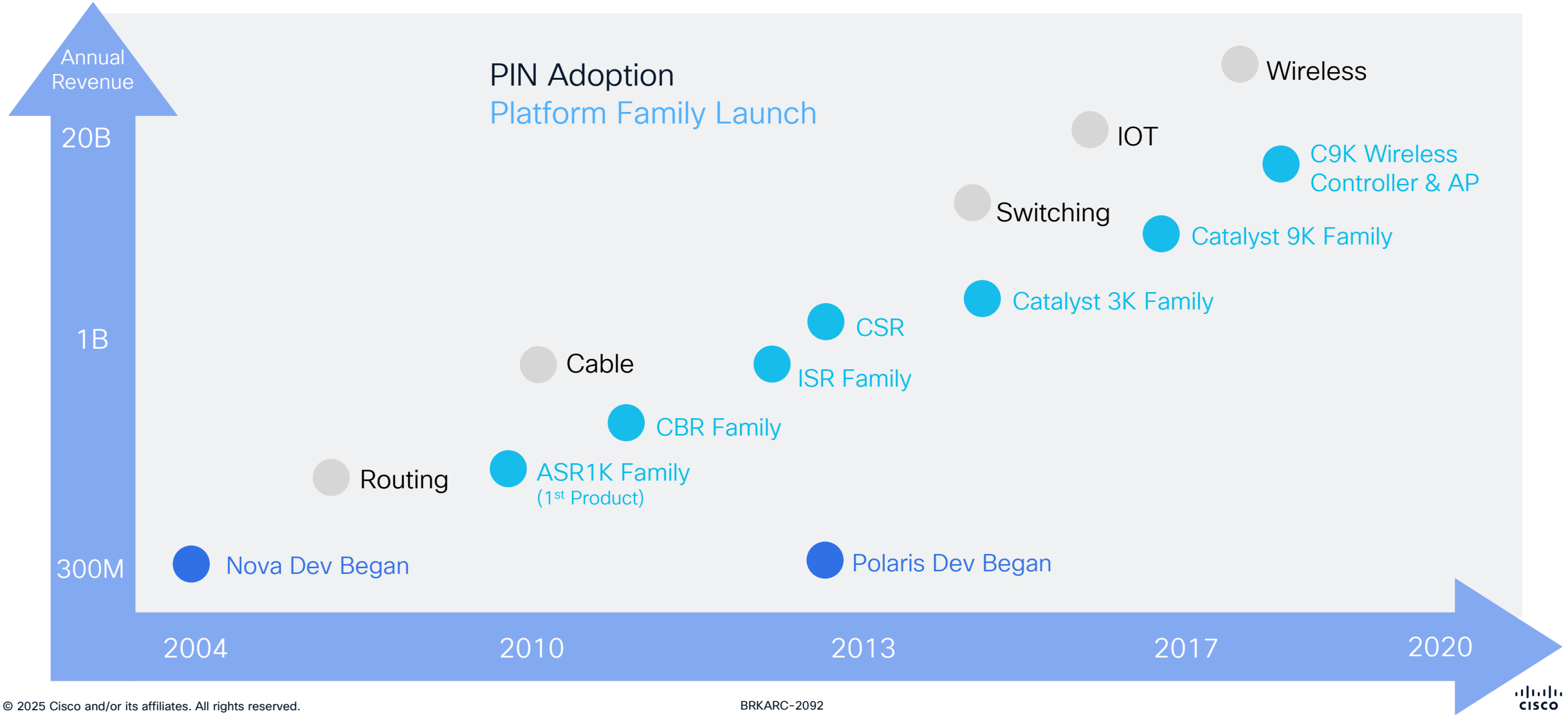







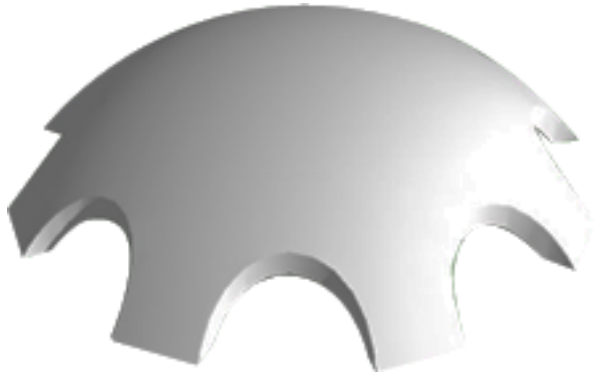
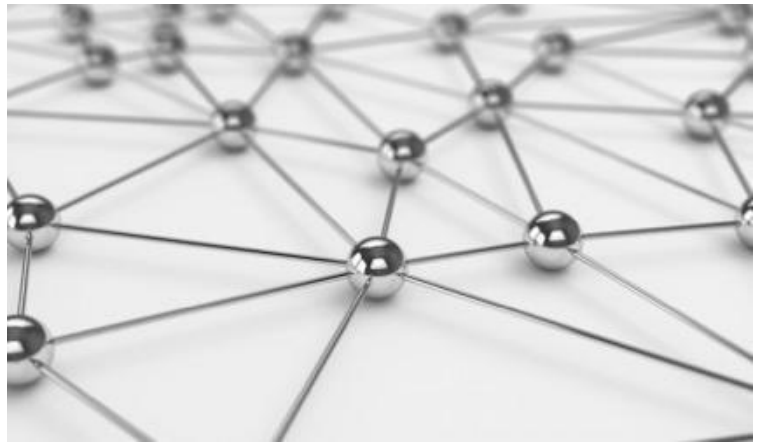

Brief History of IOS XE

Across Cisco Enterprise Platforms



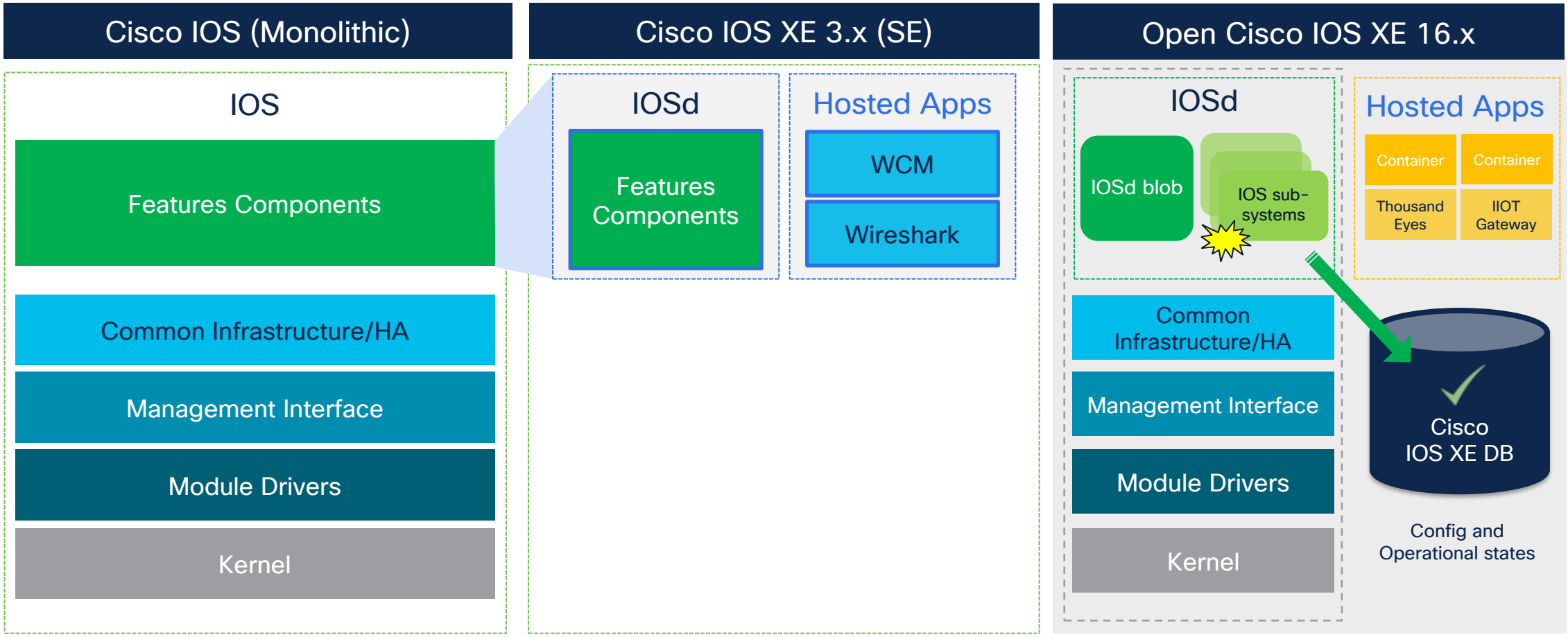
Cisco IOS XE - Architecture Evolution

Same look and feel - more powerful architecture

Cisco IOS	Cisco IOS XE 3.7.x (SE)	Cisco IOS XE 16.x
		
• **Monolithic IOS** • Compact, Streamlined • High performance	• **Monolithic IOSd**: Control-plane • Sub-packages for data plane • Linux daemons hosting capability • Message parsing capability	• **IOSd**: Component assemblies • **Modularized features**: Sub-packages • **Distributed Operating System** • **IOS XE (Crimson) Database** • Radioactive tracing and events

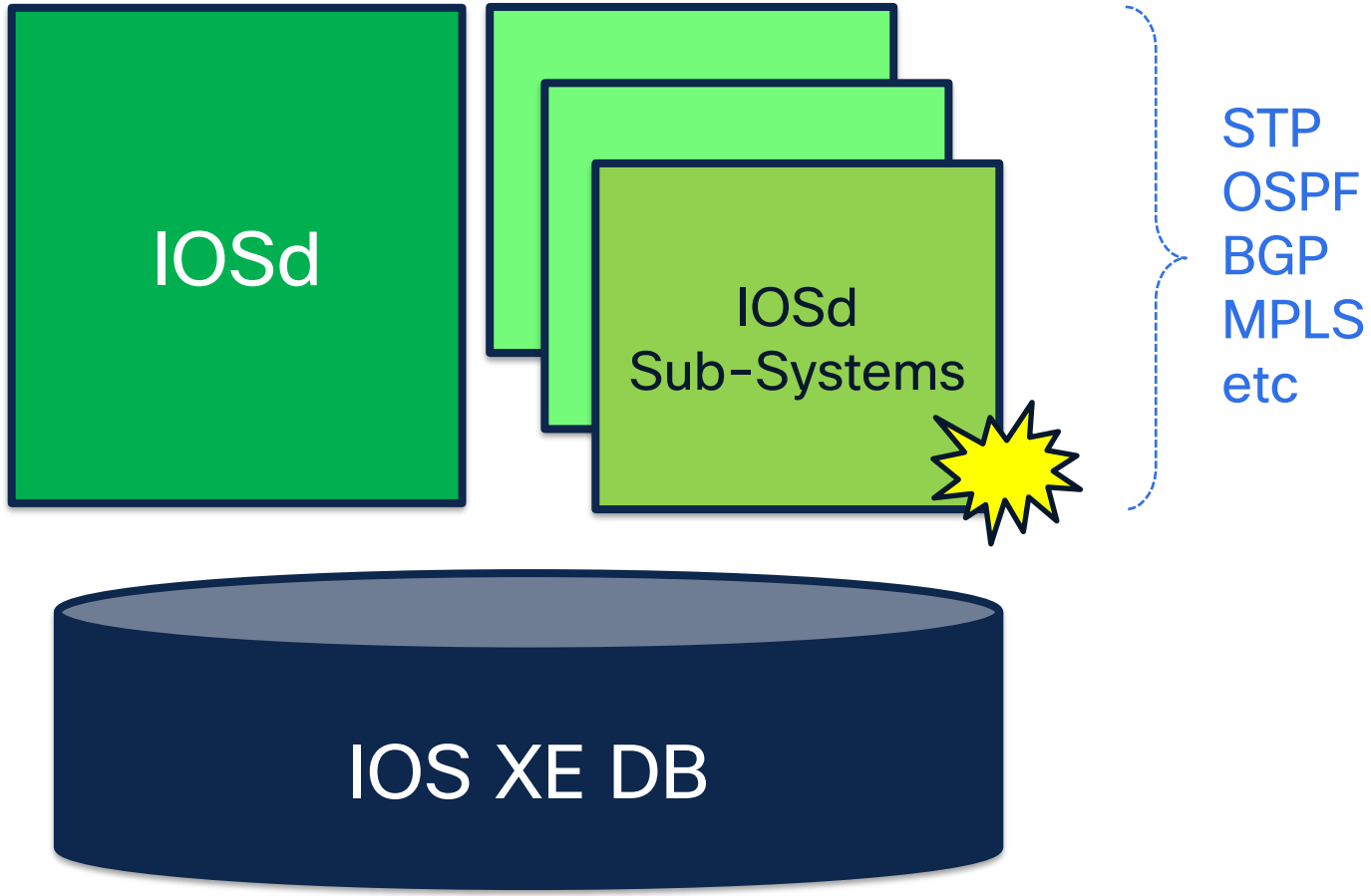
What is Cisco IOS XE?

Same look and feel – more powerful architecture



Modern Software Architecture – with the same look and feel

Cisco IOS XE – IOS Sub Systems

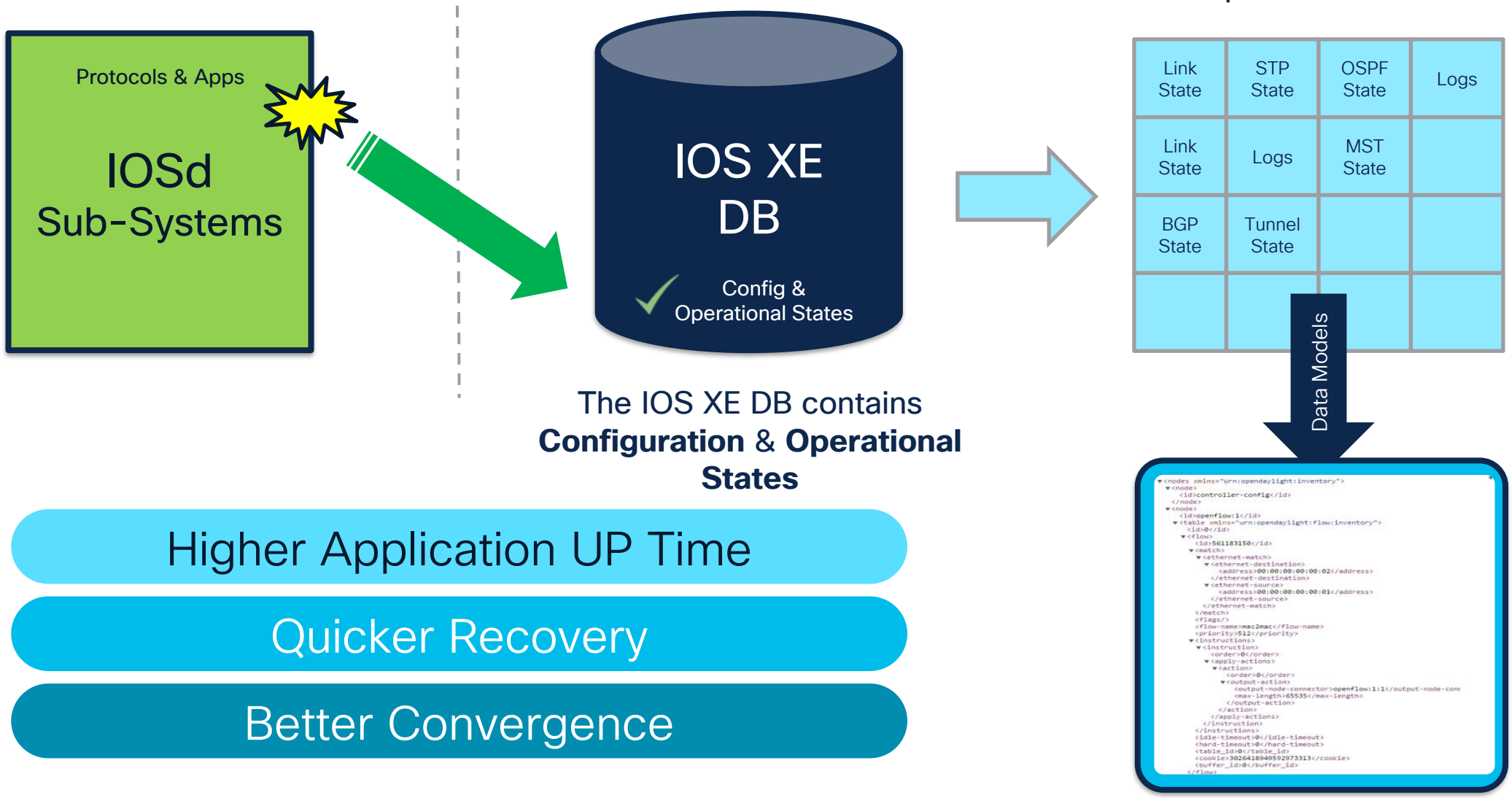


Failure of one IOS XE Sub-System(s) - keeps rest of the system intact

IOSd Sub-Systems enhance IOS Resiliency

Cisco IOS XE – Hardware DB

Decoupling Code & **Data**
protects the Configuration
& Operational States



The IOS XE DB contains
Configuration & **Operational States**

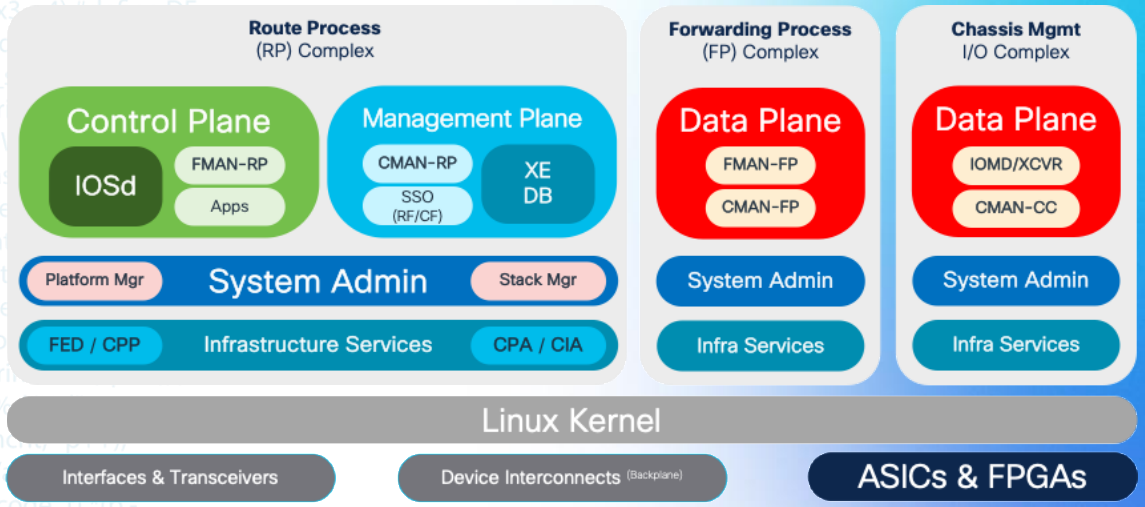
Higher Application UP Time

Quicker Recovery

Better Convergence

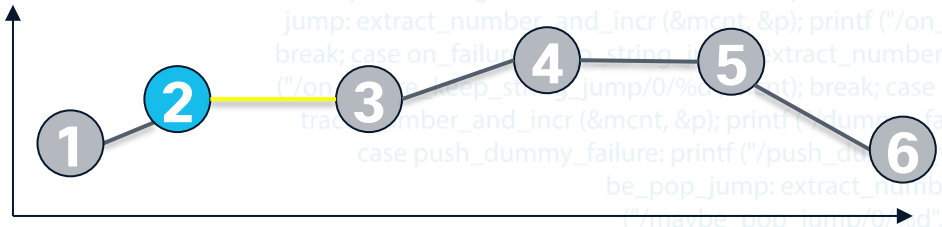
IOS XE Architecture

- Control Plane
- Data Plane
- System Plane
- Management Plane



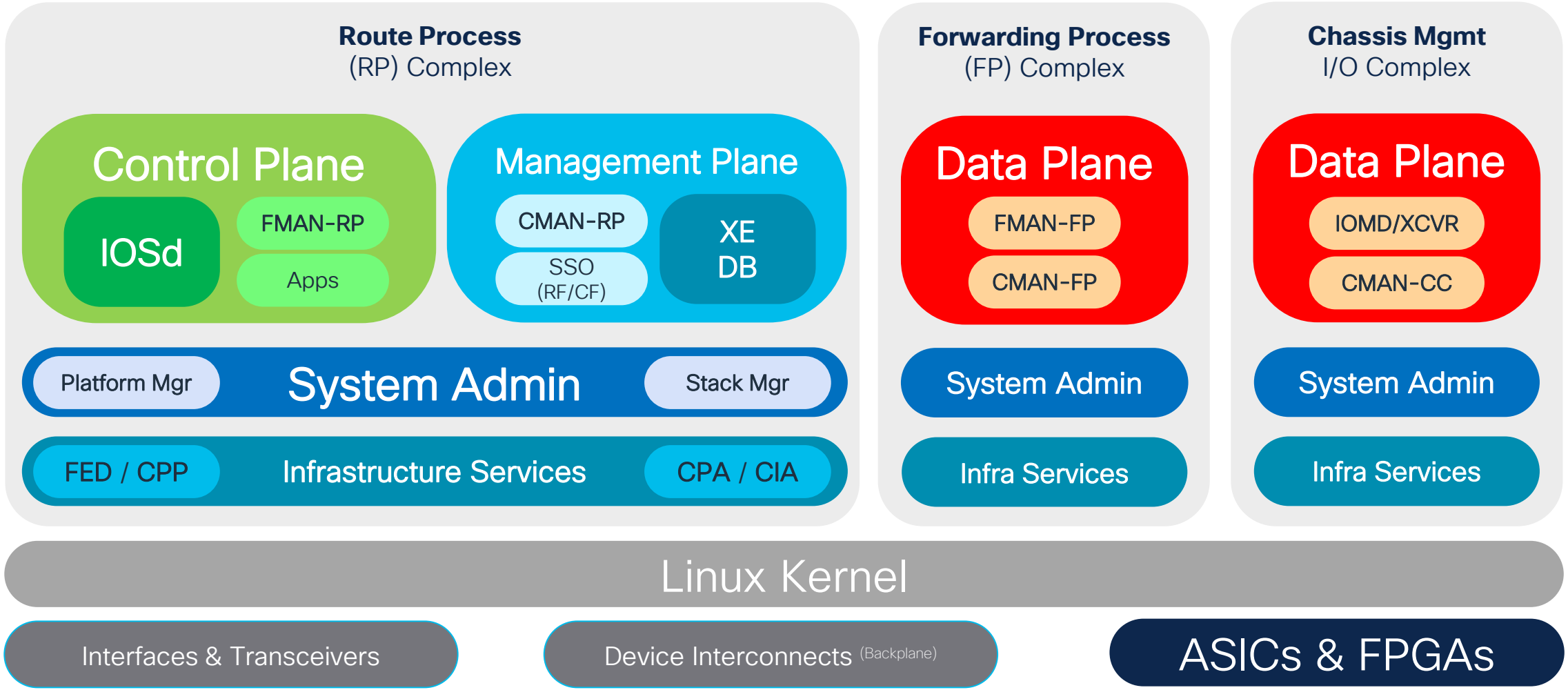
IOS XE on Cisco C9K

- IOS XE Lite



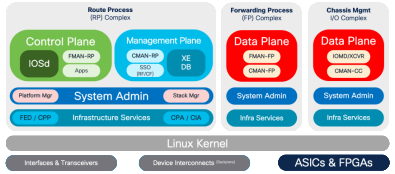
Cisco IOS XE Architecture

Modularized Components for Software Abstraction



Cisco IOS XE Software

PI vs. PD Software Components



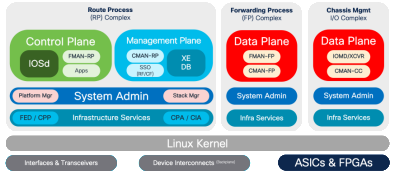
Platform Independent (PI)

- **IOS** – Internetwork Operating System
- **FMAN** – Forwarding Manager
- **RP** – Routing Process
- **FP** – Forwarding Process
- **CGM** – Classification Group Manager
- **IFM** – Interface Manager
- **AOM** – Abstract Object Manager
- **PDS** – Packet Distribution Service
- **LSMPI** – Linux Shared Memory

Platform Dependent (PD)

- **CPA** – Common Platform Abstraction
- **FED** – Forwarding Engine Driver
- **IOMD** – I/O Manager
- **CMAN** – Chassis Manager
- **PMAN** – Platform Manager
- **SMAN** – Stack Manager
- **XCVR** = Transceiver/Optics
- **Table Manager** – Client & Server
- **Punject** – Punt+Inject (CPU) interface

Cisco IOS XE - Control Plane



1 Control Plane

Data Plane

System Plane

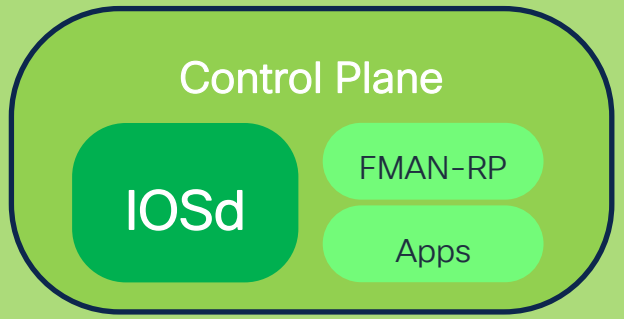
Management Plane

Infrastructure Services

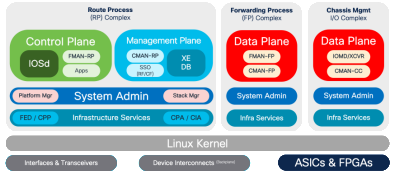
Linux Kernel & Platform Drivers

This is the 'brain' of the network stack

- Most control-plane logic runs within IOSd
- Home to routing & bridging protocols (network learning)
- Richest networking features in industry (~5000 features)
- Distributes protocol (RP) forwarding states to data-plane (FP)



Cisco IOS XE - Data Plane



Control Plane

2 Data Plane

System Plane

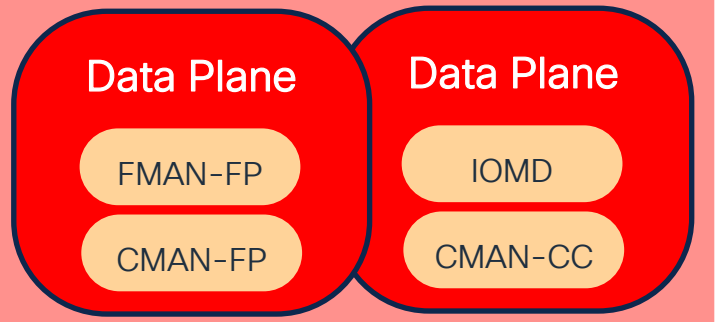
Management Plane

Infrastructure Services

Linux Kernel & Platform Drivers

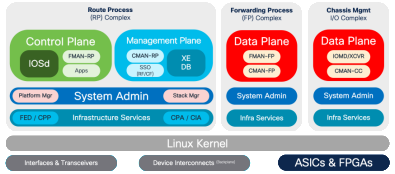
Handles high-speed Packet Forwarding

- Touches every packet! High-throughput and low-latency forwarding
- Programming from control-plane abstracted by well defined APIs
- Supports multiple forwarding architectures: standalone & modular
- Forwarding is generally handled in custom hardware (e.g. UADP & S1)



cisco

Cisco IOS XE - System Plane



Control Plane

Data Plane

3

System Plane

Management Plane

Infrastructure Services

Linux Kernel & Platform Drivers

General Administration & functions of the System

- Manages the Chassis, Modules, I/O, Power, Fans
- Manages Stacking & Virtual Chassis processing
- Also manages software image management & patching

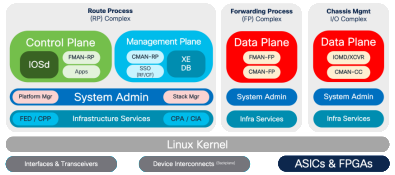
CMAN-FP | CMAN-CC | IOMD

System Admin

Platform Mgr | Stack Mgr

cisco

Cisco IOS XE – Management & Infra



Control Plane

Data Plane

System Plane

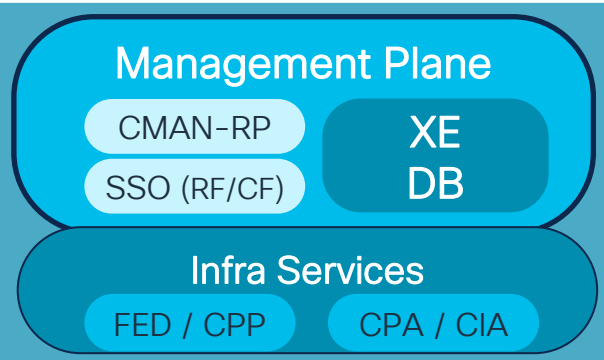
4 Management Plane

Infrastructure Services

Linux Kernel & Platform Drivers

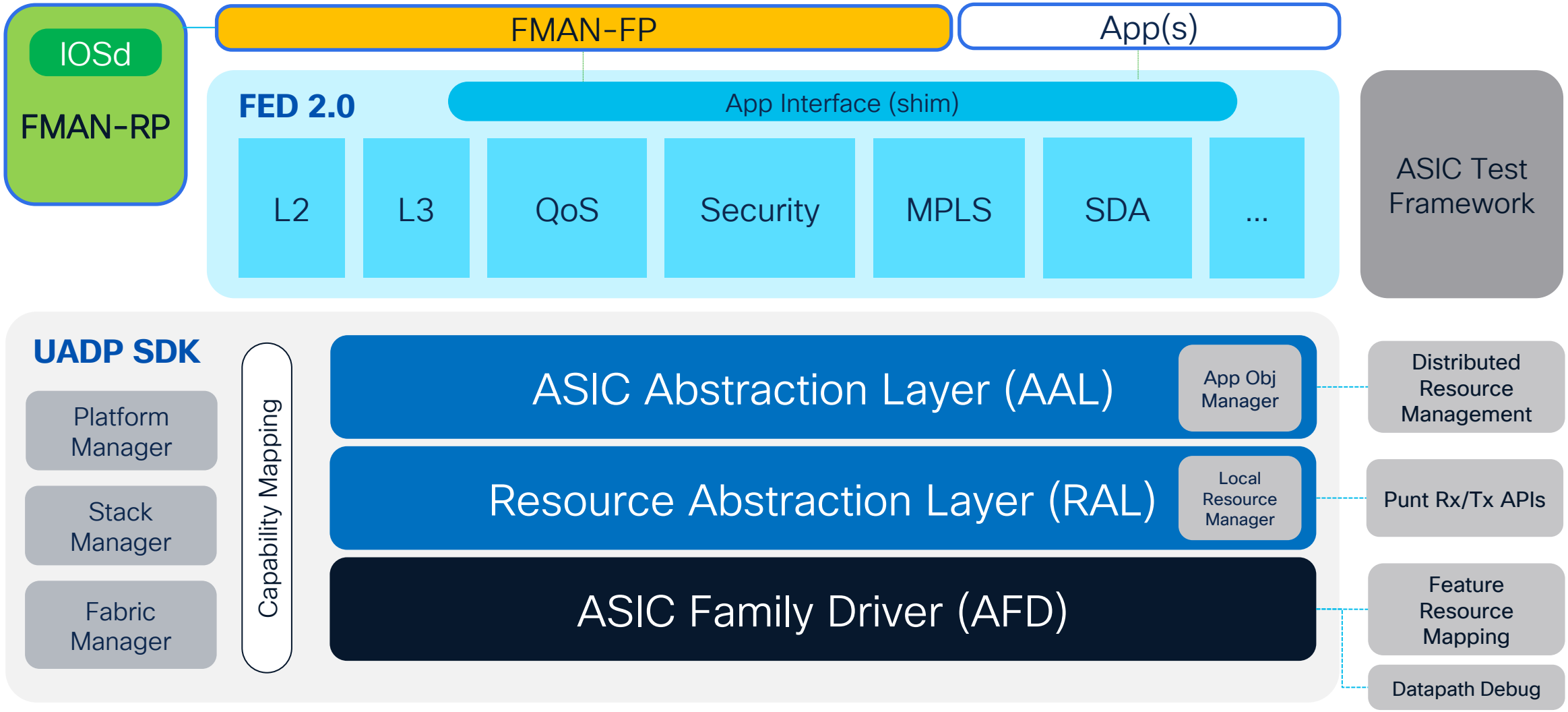
Device-Specific Services

- HA & ISSU
- Messaging
- Licensing
- XE Database
- TDL DSL
- HW Drivers
- Compiler
- Btrace
- Buildtime tools

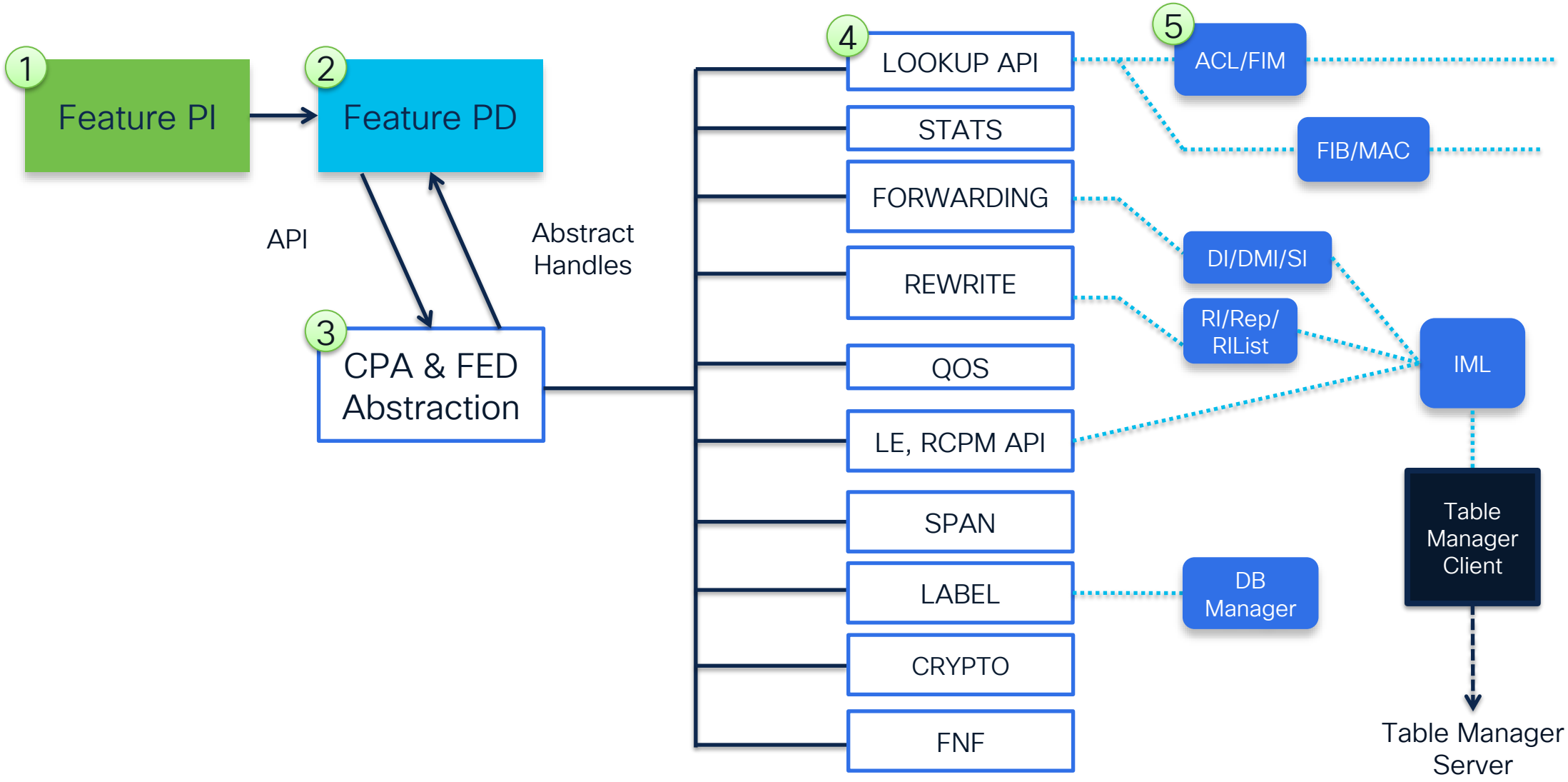


Cisco IOS XE on Catalyst 9000 Series

Hardware Forwarding Architecture



Cisco IOS XE – PD Abstraction Layer



Cisco IOS XE “Lite” Architecture

Same code base as Cisco IOS XE – Optimized for ARM CPU & Memory

Route Process
(RP) Complex

Control Plane

IOSd

FMAN-RP

Apps

Management Plane

CMAN-RP

SSO
(RF/CF)

XE
DB

Stack Mgr

Infrastructure Services

Forwarding Process
(FP) Complex

Data Plane

FMAN-FP

FED

Infra Services

Chassis Mgmt
I/O Complex

Data Plane

IOMD-Lite

Infra Services

Linux Kernel

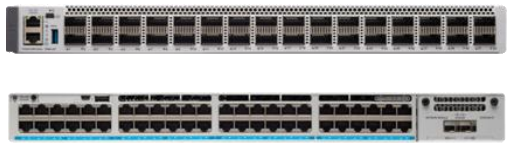
Interfaces & Transceivers

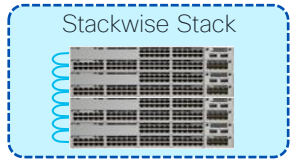
Device Interconnects (Backplane)

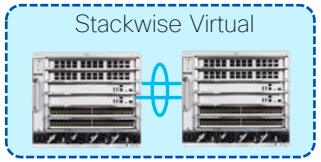
ASICs & FPGAs

Fixed vs. Modular vs. Stacking

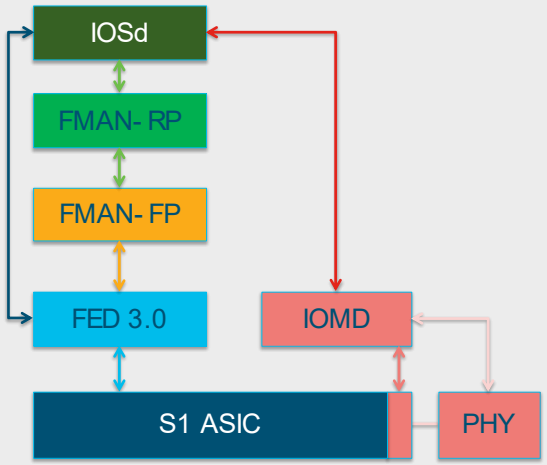
Reusing Common Elements of OS Architecture



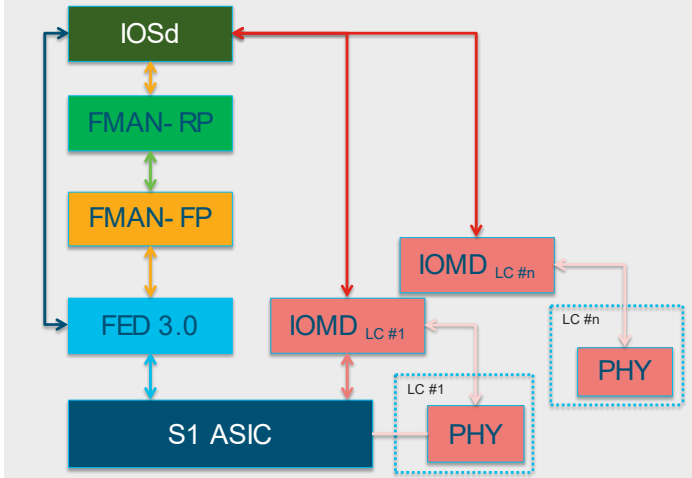




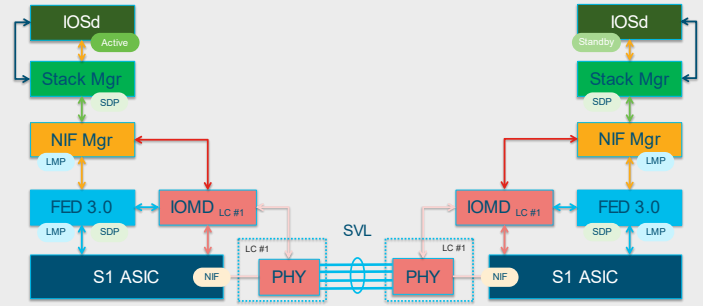
Fixed Platform



Modular Platform

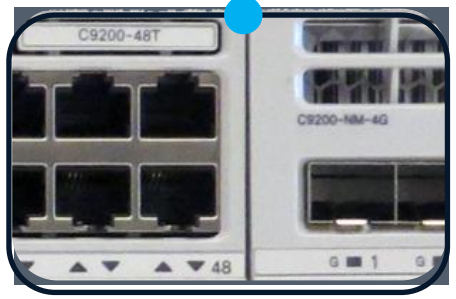


Stacked Platform(s)

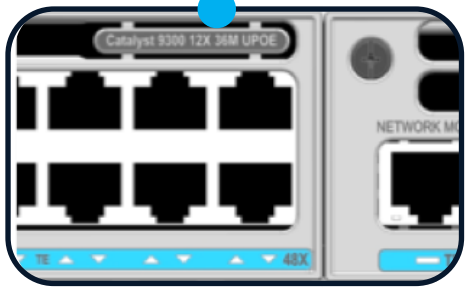


Cisco IOS XE

16.x - 17.x



Catalyst 9200/L/CX



Catalyst 9300/L/X

Catalyst 9400/X

Catalyst 9500/X

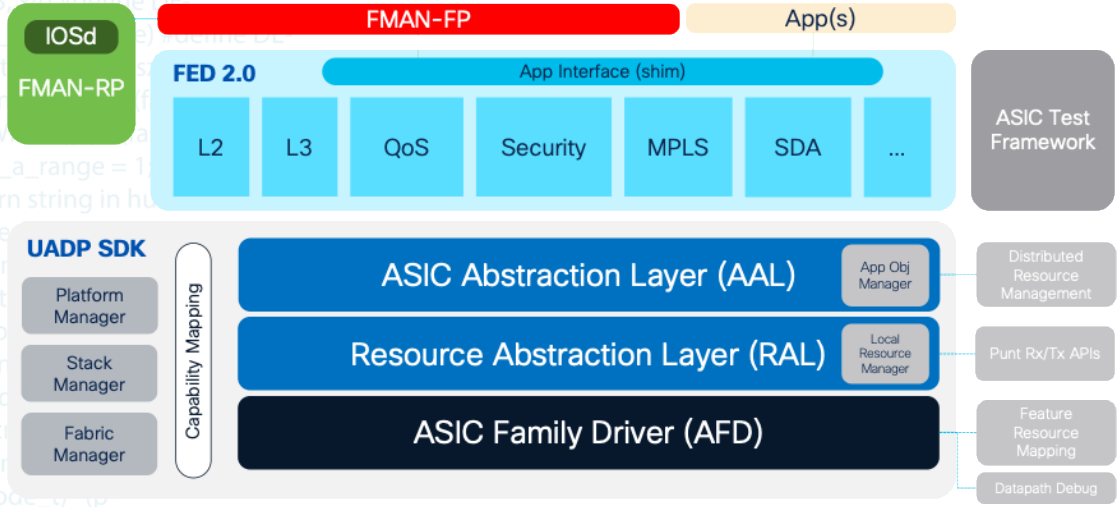
Catalyst 9600/X

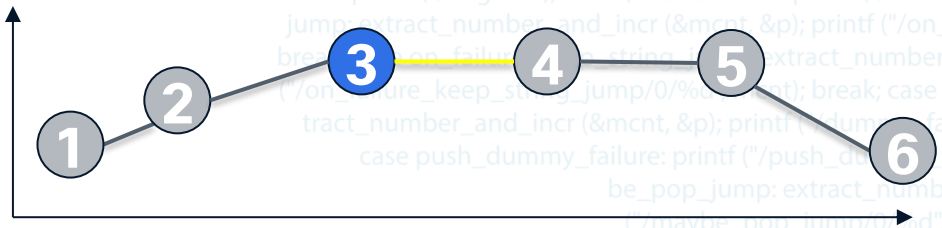
IOS XE Lite
Binary Image

IOS XE
Binary Image

Catalyst 9000 runs the same IOS XE Operating System

- Existing C9K Portfolio
- IOS XE Release Model
- IOS XE 17.1.1 – 17.6.1
- IOS XE 17.7.1 – 17.15.1

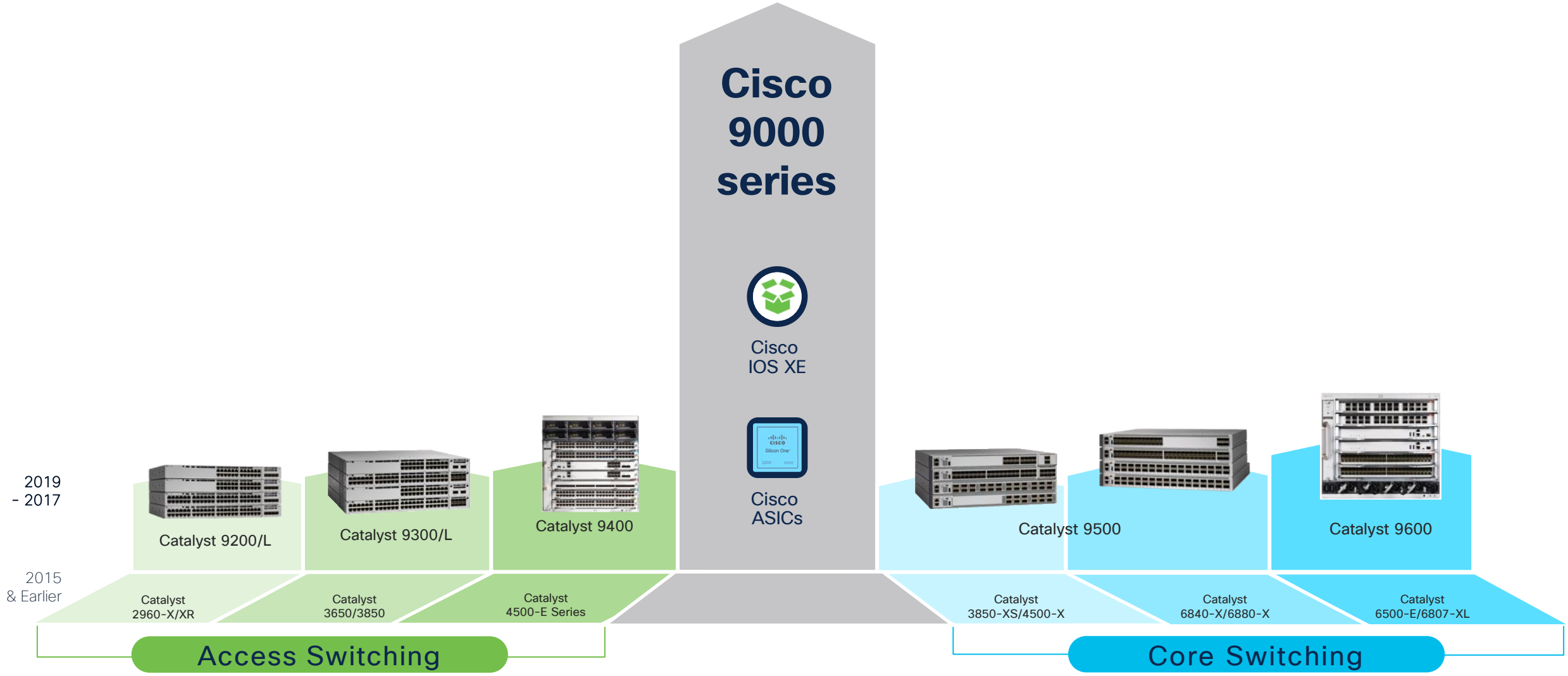




Cisco Catalyst 9000 Switching Portfolio

One Family from Access to Core – Common Hardware & Software

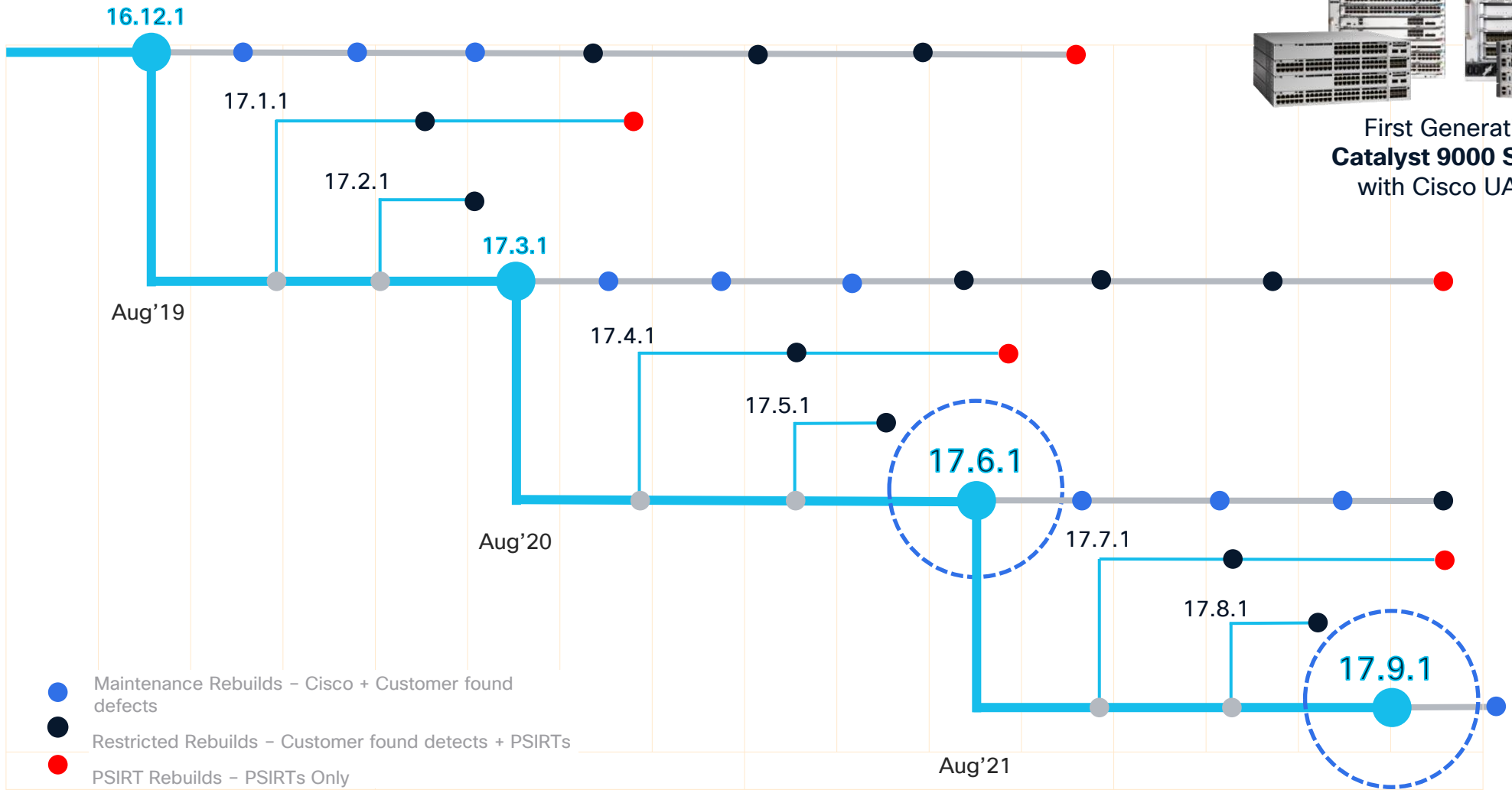
16.6.x – 17.6.x



Cisco IOS XE – Release Schedule

Graphical Overview – 17.1.x to 17.9.x

First Generation
Catalyst 9000 Series
with Cisco UADP



Catalyst 9000 Switching – Key Features

Reference

* Limited Availability (LA) only

IOS XE 17.1.1 (Dec'19) SMR	IOS XE 17.2.1 (Apr'20) SMR	IOS XE 17.3.1 (Aug'20) EMR
Enhanced Security ❖ 9200/9300 – Umbrella Integration ❖ MACSEC over EoMPLS ❖ ERSPAN to v6 Destination	**Enhanced Security** ❖ TWS – Secure Swipe Clean DoD 5220.22-M standard	**Enhanced Security** ❖ Enhanced ACL Logging ❖ Wired Client Sensor* ❖ 9200/9300 – Umbrella Switch Connector with AD Integration
Overlays & Segmentation ❖ Inter-AS Option A (VRF-Lite) ❖ VPLS Flow Aware Transport (FAT) PseudoWire ❖ Extranet mVPN ❖ VXLAN aware Flexible Netflow ❖ EVPN to VRF-Lite handoff for Border Spine ❖ EVPN to MPLS handoff for Border Spine ❖ EVPN Tenant Routed Multicast (TRM)	**Overlays & Segmentation** ❖ EVPN – VxLAN ARP/ND flooding suppression. ❖ EVPN to MPLS hand off on Cat9K in Border spine role (single box) ❖ Hierarchical VPLS ❖ VPLS Multiple VCs per Spoke	**Overlays & Segmentation** ❖ mLDP: Multicast LDP* ❖ VPLS Routed PseudoWire (IRB): IPv6 Unicast ❖ MVPNv6 (Multicast 6VPE) ❖ MPLS VPN – Inter-AS Option AB ❖ BGP EVPN w VxLAN BUM rate-limiting support ❖ BGP-EVPN w VXLAN MAC/IP learning on Access ❖ Wide Area Bonjour with BGP-EVPN over VXLAN
Forwarding & Features ❖ 9600 – VRF aware PBR ❖ 9400 – NAT Profile	**Forwarding & Features** ❖ NAT – VRF aware NAT (VRF to Global)	**Forwarding & Features** ❖ 9500H/9600 : Customized SDM Template Ph1 (FIB) ❖ IP-FRRv4: LFA EIGRP and OSPFv2 per prefix ❖ Non-Stop Routing (NSR): L3 Forwarding Redundancy ❖ LACP 1:1 redundancy and dampening
High Availability ❖ 9600 – Quad Sup SVL Support (RPR) ❖ 9300 – xFSU Standalone	**High Availability** ❖ 9300 – xFSU reload with backside stacking* ❖ 9300 – xFSU support with dot1x, MAB, Webauth* ❖ 9300 – xFSU : LACP Protocol support*	**High Availability** ❖ Flexlink+ with VLAN Load Balancing ❖ 9300 – xFSU Reload: Stacked and Standalone (17.3.2)
Platform & Programmability ❖ Per port MTU support ❖ 9500H/9600 – Unified Port Buffer ❖ 9400 – Native Docker for App Hosting	**Platform & Programmability** ❖ 9400 – 9216 bytes MTU ❖ 9600 – Breakout Support ❖ gPTP/ PTPv2 support on Port Channels	**Platform & Programmability** ❖ PVLAN on Trunks and Port Channels ❖ PTPv2 and gPTP support on 9400* ❖ ETA and AVC Interoperability on same port ❖ SHA-512 secure image-bootup integrity check ❖ gRPC Model Driven Telemetry (MDT) with TLS
Hardware & Optics ❖ **C9300L** mGig SKUs ❖ **C9600-LC-48TX** mGig Linecard	**Hardware & Optics** ❖ **9500/9600** – AOC/DAC, QSFP-4SFP10G	**Hardware & Optics** ❖ None

www.cisco.com/c/en/us/products/collateral/ios-nx-os-software/ios-xe-17/ios-xe-17-6-x-eol.html

Catalyst 9000 Switching – Key Features

Reference

* Limited Availability (LA) only

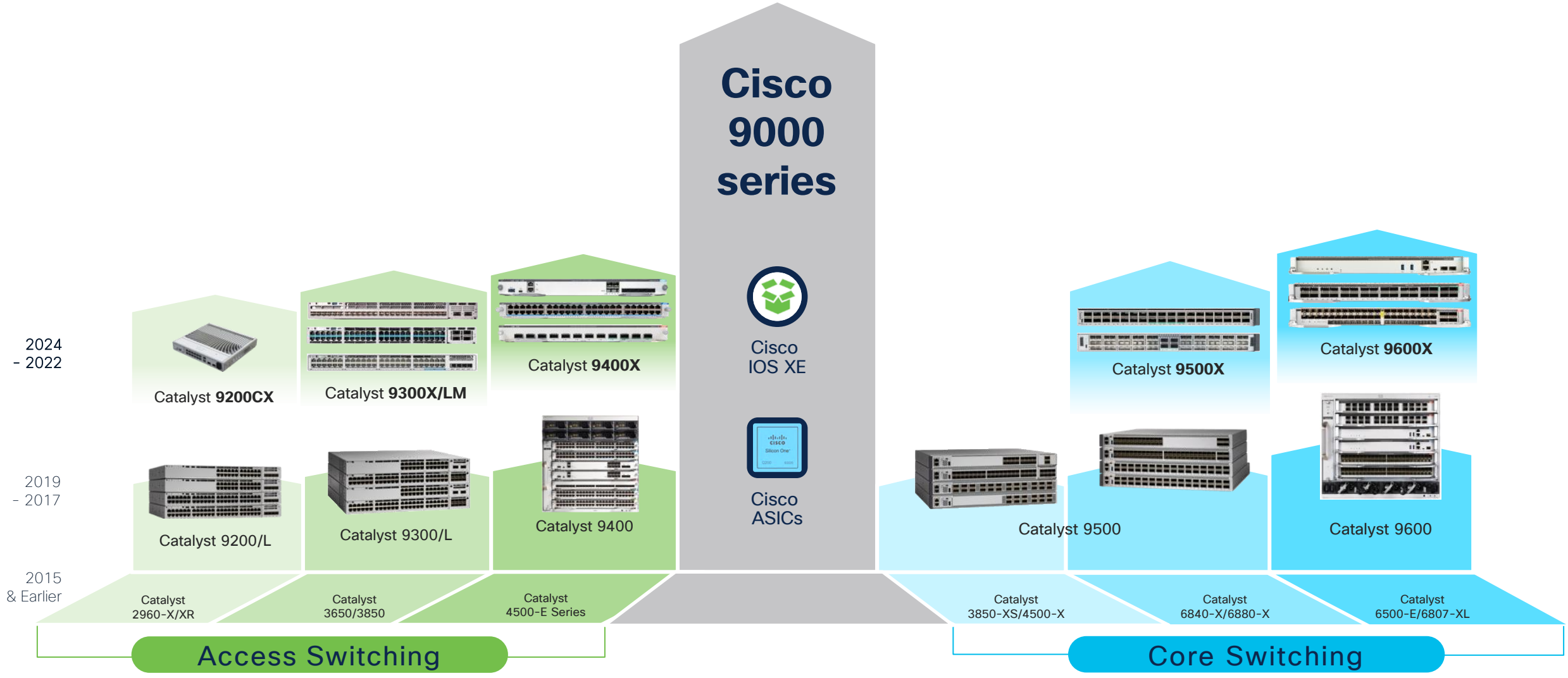
IOS XE 17.4.1 (Nov'20) SMR	IOS XE 17.5.1 (Apr'21) SMR	IOS XE 17.6.1 (Aug'21) EMR
Enhanced Security ❖ FQDN ACLs ❖ RADSEC – Radius over TLS and DTLS ❖ Stealthwatch Cloud Integration* ❖ Wired Client Sensor with Flash*	**Enhanced Security** ❖ FQDN Redirect ACL ❖ Wired Dynamic VLAN ❖ Secure Network Analytics Connector ❖ DSCP Marking for RADIUS Packets ❖ Session timers AV Pair ❖ Interface Templates ❖ Trustworthy Systems	**Enhanced Security** ❖ 9300X – IPsec Phase1 – SVTI, IKEv2 ❖ IPv6 FQDN Redirect ACL ❖ RADSEC CoA Enhancement
Overlays & Segmentation ❖ PVLAN with BGP EVPN over VxLAN	**Overlays & Segmentation** ❖ Selective Q-in-Q ❖ BGP EVPN L2/L3 VNI scale	**Overlays & Segmentation** ❖ MPLS Traffic Engineering (TE) – Phase1 ❖ LACP/PAGP over EoMPLS ❖ MLD snooping over VPLS
Forwarding & Features ❖ 9500H/9600 – Customized SDM Template Ph2 (ACL)	**Forwarding & Features** ❖ 9500H/9600 – Customized SDM Template Ph3 (4K VLAN) ❖ Enhanced NAT scale ❖ BGP Monitoring Protocol ❖ WCCP Over GRE	**Platform Features** ❖ VRF Aware WCCP ❖ Enhanced NAT Session Monitoring ❖ NAT Precedence ❖ Bonjour mDNS SSO, FHRP Service Peer Support
High Availability	**High Availability**	**High Availability** ❖ VRRPv3 SSO
Platform & Programmability ❖ YANG model updates ❖ Smart Licensing using Policy	**Platform & Programmability** ❖ gPTP over L3 Unicast ❖ Disable USB SSD ❖ App Hosting Updates	**Platform & Programmability** ❖ App Hosting on 9300X ❖ Thousand Eyes – 4.0 Version Agent ❖ Perpetual PoE/UPOE with StackPower ❖ PTP on StackWise*, PTP over SDA ❖ Programmability & Automation updates
Hardware & Optics ❖ **9500H/9600** – SFP-10G-TX, QSFP-40/100-SR4, ❖ **9600** – 4 x 25G Breakout, GLC-GE-100FX and GLC-TE-100M	Hardware & Optics ❖ **C9400-LC-48HN** – 5G MGIG line card with 90W PoE	**Hardware & Optics** ❖ **C9300X-12Y / 24Y** – 10/25G Fiber Switch with Cisco UADP2.0sec ❖ **C9300X-NM** – 2x 40/100G, 8x 10/25G, 8x mGiG uplinks

www.cisco.com/c/en/us/products/collateral/ios-nx-os-software/ios-xe-17/ios-xe-17-6-x-eol.html

Cisco Catalyst 9000 Switching Portfolio

One Family from Access to Core – Common Hardware & Software

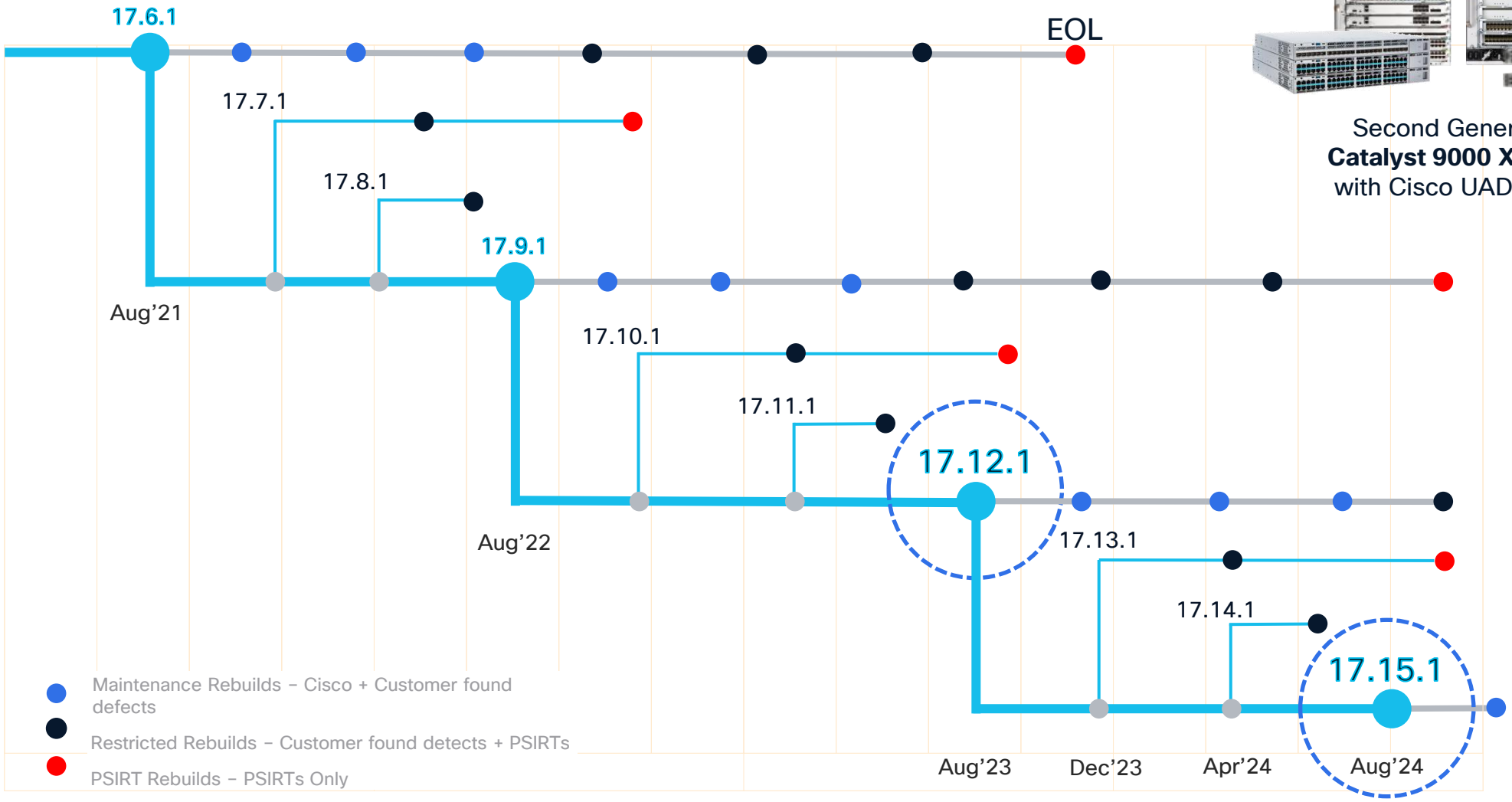
17.7.x – 17.15.x



Cisco IOS XE – Release Schedule

Graphical Overview – 17.7.x to 17.15.x

Second Generation
Catalyst 9000 X Series
with Cisco UADP & S1



C9K IOS XE 3.0 – Highlights

Secure

- Secure Boot, Image Signing
- SELinux, X.509

Zero Copy Punt

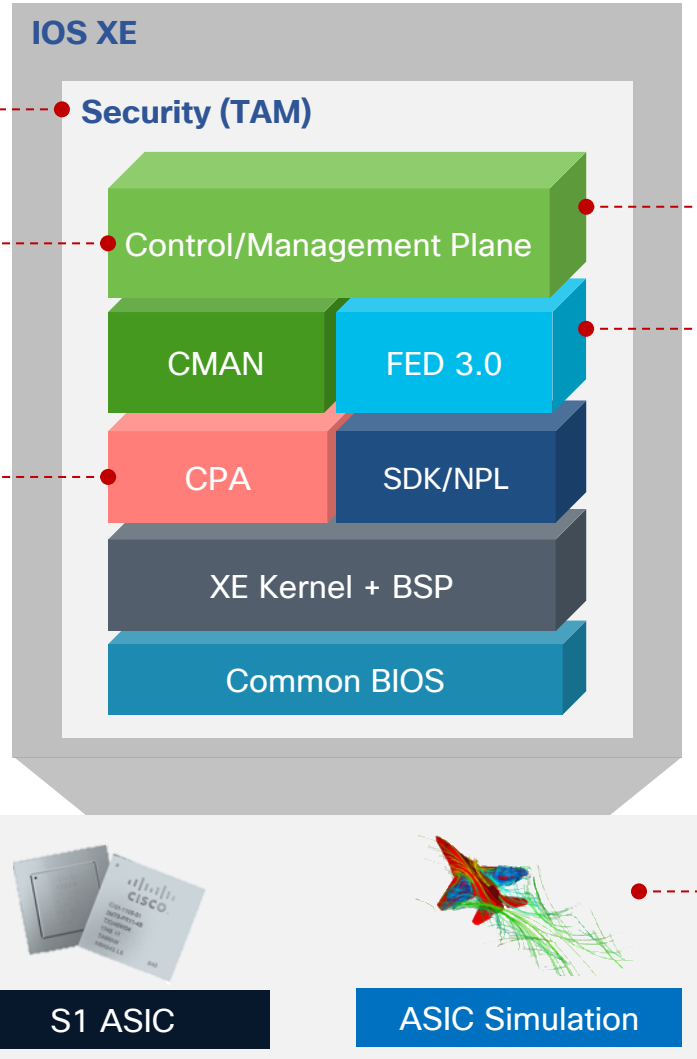
- High Speed zero-copy punt to enable Software-based Apps (e.g. NetFlow)

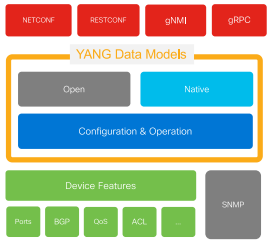
CPA – Single Source of Truth, HW Abstraction

- CPA architecture for sharing common software across multiple platforms
- Single Source of Truth – for various devices and interconnects

Custom Cisco ASIC + SDK

- High capacity, programmable ASIC
- Common SDK as an integration layer





Programmable

- Managed Through Models
- Programmable through YANG

FED3.0 – Model Driven Forwarding

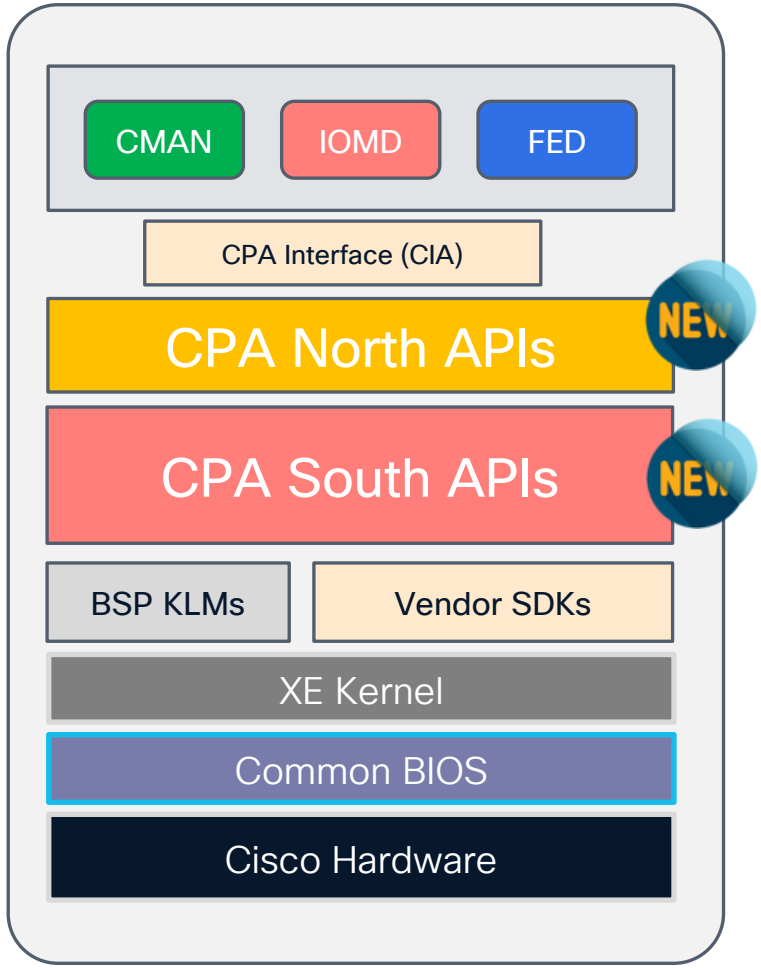
- Bring Polaris infrastructure to FED
- Bring FED closer for stateful restart

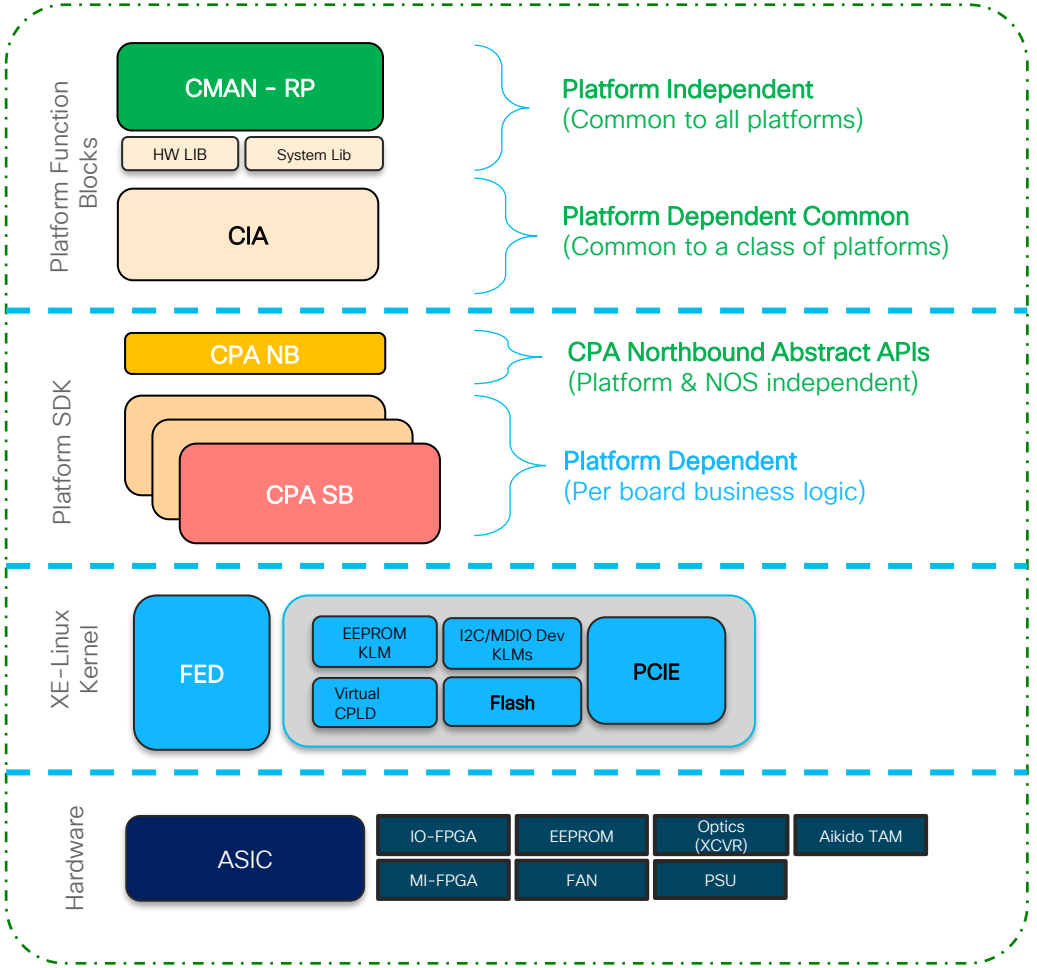
SPECTRA

- Integrated ASIC SDK/NPL Testing

C9K IOS XE 3.0 – Platform Infra

Architecture Evolution – Common Platform Abstraction (CPA)





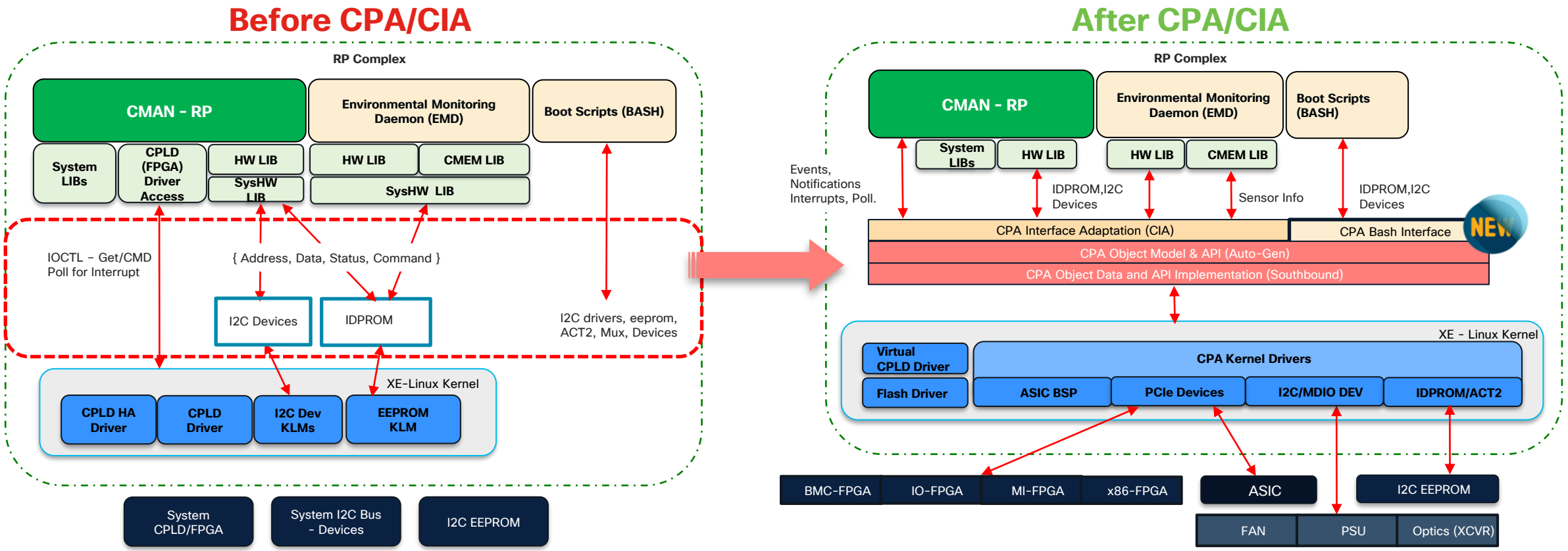
Leveraged by NG Platforms

PD code

C9K NG IOS XE- CPA Overview

Architecture Evolution – before & after

Cisco Platform Abstraction (CPA) is a model-driven HW to SW disaggregation layer for platform devices. It hides board and device connection details from upper-layers of platform features - acts as a “single source of truth” for hardware data.

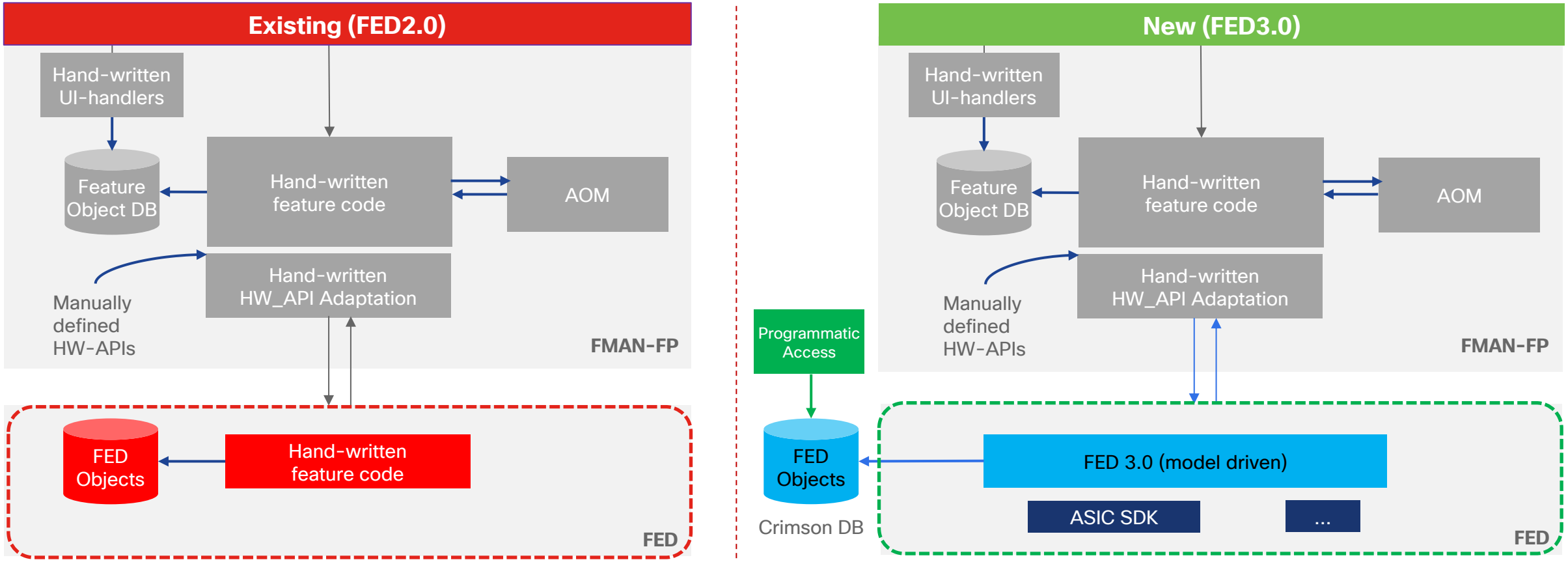


CPA provides common & consistent inventory and device-access helper functions (APIs) for admin-plane features

C9K NG IOS XE – FED 3.0 Overview

FED 3.0 - Before & After

IOS XE and FED have been enhanced to support various types of databases and to support automatic code-generation

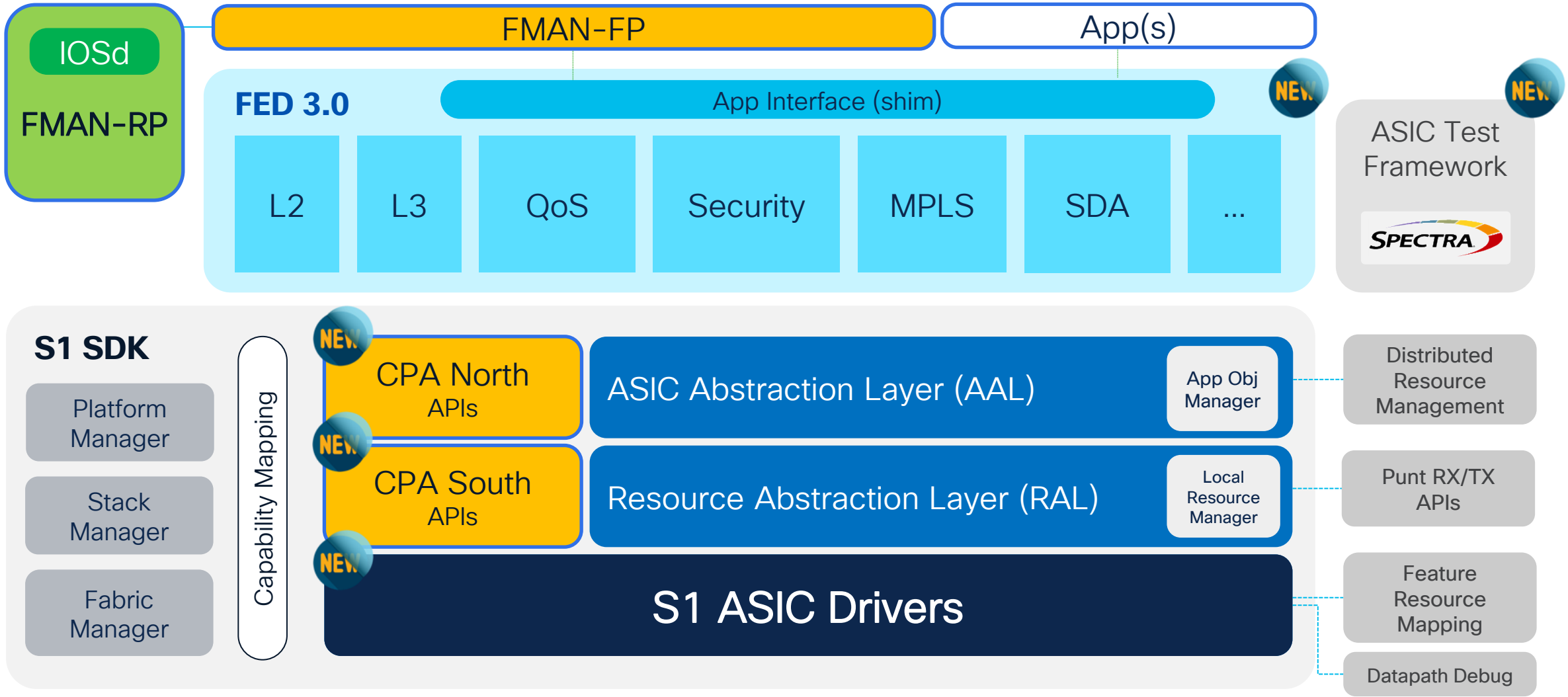


- Controller visibility of HW forwarding objects
- Time series for HW forwarding objects
- Stateful restart HW forwarding objects
- Automatic code-generation for object life-cycle

Manual
Auto-generated
New capability

C9K NG IOS XE – Overview

Platform Forwarding Architecture

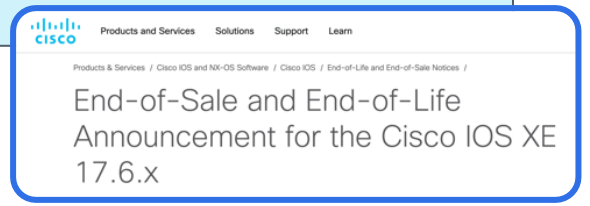


Catalyst 9000 Switching – Key Features

Reference

* Limited Availability (LA) only

IOS XE 17.7.1 (Dec'21) SMR	IOS XE 17.8.1 (Apr'22) SMR	IOS XE 17.9.1 (Aug'22) EMR
Enhanced Security ❖ 9500X/9600X – MACsec ❖ 9200/9300 – API Registration for Umbrella Switch connector	**Enhanced Security** ❖ 9300X – IPsec Phase2 – Multicast (SVTI) ❖ 9500X/9600X – WAN-MACsec, with HSEC license ❖ SW SUDI 2099 Enablement	**Enhanced Security** ❖ 9300X – IPsec Phase3 – NAT Traversal ❖ 9300X – VRF-aware IPsec ❖ Reflexive ACL
Overlays & Segmentation ❖ 9500X/9600X – MPLS and TE Phase1 ❖ 9500X/9600X – EoMPLS ❖ EVPN L3 TRM with MDT Data	**Overlays & Segmentation** ❖ EVPN L2 TRM	**Overlays & Segmentation** ❖ SDA LISP Graceful Restart for MAC cache ❖ SDA VN Extranet across SDA Transit
Forwarding & Features ❖ 9500X/9600X – L3 Routing (IGP, BGP) feature set ❖ Low priority Control packet mapping to Non-LLQ ❖ Bonjour – Micro-Location services	**Forwarding & Features** ❖ 9500X/9600X – Sampled Flexible NetFlow	**Forwarding & Features** ❖ Destination IP NAT scale enhancement ❖ PAT support for Enhanced NAT scale ❖ Conditional Static NAT using Route-map
High Availability ❖ 9400X/9600X – SSO & ISSU ❖ 9300X – xFSU	**High Availability** ❖ 9500H/9600 – Graceful Insertion & Removal (GIR)	**High Availability** ❖ 9400X – StackWise Virtual (Dual-Sup)
Platform & Programmability ❖ PTP on 9300 StackWise ❖ PTP on 9600 ❖ PTP AES67 compliance ❖ AVNU Certification – 9300 & 9500 ❖ gNOI reset.proto – tooling	**Platform & Programmability** ❖ PTP – G8275.1 ITU Telcom Profile on 9300/9300X ❖ 9500X/9600X – L3 Sub-Interface Queuing ❖ C9300 System Power-Consumption Reporting ❖ gNMI Native Configuration Yang Model ❖ Guest Shell HA – Guest-Share Folder Sync	**Platform & Programmability** ❖ 9500H – AVB support ❖ 9400X – Perpetual PoE support ❖ 9400X – Support for hosting multiple applications ❖ 9400X – 432 Port-Channels ❖ 9400X – 4K VLANs support
Hardware & Optics ❖ **C9300X-48TX / 48HX** – 48x mGig Switch (Cisco UADP2.0sec) ❖ **C9400X-SUP-2/XL** – Supervisor 2 (Cisco UADP3.0sec) ❖ **C9500X-28C8D** – 100/400G Fiber switch (Cisco S1 Q200) ❖ **C9600X-SUP-2** – Supervisor 2 (Cisco S1 Q200) ❖ **C9600-LC-40YL4CD** – 40x SFP + 4x QSFP Combo Linecard	**Hardware & Optics** ❖ **C9400-LC-48HX** – 48x mGig Linecard ❖ **C9400-LC-48XS** – 48x 1/10G Linecard ❖ **C9600-PWR-3KW** – 3000W AC PSU	**Hardware & Optics** ❖ **C9200CX** – 12x Compact switch (Cisco UADP2.0mini) ❖ **C9300LM** – 24/48x + Fixed Uplinks, ≤14 in. (Cisco UADP2.0sec) ❖ **C9600-LC-32CD** – 32x 100G / 24x 100G + 2x 400G QSFP Linecard



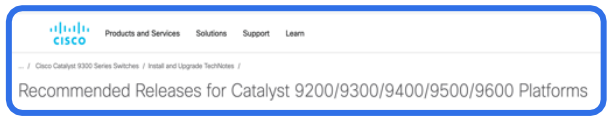
www.cisco.com/c/en/us/products/collateral/ios-nx-os-software/ios-xe-17/ios-xe-17-9-x-eol.html

Catalyst 9000 Switching – Key Features

Reference

* Limited Availability (LA) only

IOS XE 17.10.1 (Dec'22) SMR	IOS XE 17.11.1 (Apr'23) SMR	IOS XE 17.12.1 (Aug'23) ^ EMR
Enhanced Security ❖ DHCP Snooping Glean ❖ Reflexive ACL for IPv4 ❖ MACsec Transparent Pass-Through ❖ Secure Data Wipe (NIST 3-pass) ❖ 9400X – IPsec support	**Enhanced Security** ❖ 9300X - GRE over IPsec support ❖ 9400X - NAT-Traversal support for IPSEC ❖ 9500X/9600X - IPv6 SGACL support	**Enhanced Security** ❖ IC2M updates for FIPS 140-3 ❖ IPSEC OSFPv3 Auth support ❖ Service Redirect (Firewall PBR) ❖ 9500X-60L4D – IPsec support (P1*)
Overlays & Segmentation ❖ BGP EVPN over IPv6 Underlay* ❖ BGP EVPN Dynamic Peering ❖ BGP EVPN over IPsec - TRM support	**Overlays & Segmentation** ❖ BGP EVPN Micro-segmentation (VLXAN-GPO) ❖ BGP EVPN Mobility-Convergence enhancements* ❖ 9500X/9600X - BGP EVPN with SVL support ❖ 9500X/9600X - MPLS VPN - Inter-AS Option A ❖ 9500X/9600X - L2VPN (EoMPLS) Pseudowire Redundancy	**Overlays & Segmentation** ❖ BGP EVPN (VRF Aware) with Dynamic NAT64 ❖ BGP EVPN Config and Operation CLI simplicity ❖ Increased VNI Scale for EVPN ❖ 9500X/9600X – EVPN L2 TRM support
Forwarding & Features ❖ Stateful NAT64 ❖ NAT on L3 EtherChannel ❖ LACP Standalone Mode on L3 EtherChannels ❖ PTPv2 on StackWise Virtual ❖ 9500X/9600X - Bonjour & mDNS Routing	**Forwarding & Features** ❖ 9500X/9600X - Policy Based Routing (PBR) ❖ 9200/9200CX – Bonjour Service Peer	**Forwarding & Features** ❖ PTPv2 on 9400X
High Availability ❖ 9500X/9600X - StackWise Virtual (Dual Sup SSO)	**High Availability** ❖ StackWise Virtual (Dual Sup SSO) on 9500X-60L4D	**High Availability** ❖ Standby Port Delay for SVL Bringup
Platform & Programmability ❖ ERSPAN on AppGig interface ❖ YANG 1.1 Support ❖ YANG Config Model support for native gNMI ❖ Guest Shell HA Guest-Share Folder Sync	**Platform & Programmability** ❖ 9400X - Customized SDM Template ❖ 9500X/9600X – ERSPAN ❖ YANG Oper model support for PTPv2 and AVB ❖ Switching Telemetry for Cisco DNA Center*	**Platform & Programmability** ❖ EPC Support of AppGigabitEthernet ❖ Upgrade firmware (CPLD/FPGA/Rommon) with IOSXE in single reload ❖ Bootup time enhancements
Hardware & Optics ❖ **C9500X-60L4CD** – 60x 50G + 4x 400G switch (Cisco S1 Q200) ❖ 9600X - 50G SFP Linecard support	**Hardware & Optics** ❖ **9500X/9600X** – Embedded-PHY 1G SFP support * ❖ Support for QSFP-100G-FR-S ❖ Support for SFP-10/25BXD-1 and BXU-1 ❖ Support for QSFP-4x10G on 100G PSM4	**Hardware & Optics** ❖ **C9400-LC-24XY** - 24x 10/25G Linecard ❖ **C9400-LC-12QC** - 12x 40/100G Linecard ❖ **C9200CX-12PD-2X2G** & **8PD-2G** ❖ 9500X/9600X - 50G SR-S/SL/Multirate support



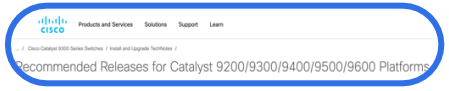
www.cisco.com/c/en/us/support/docs/switches/.../214814-recommended-releases-for-catalyst-9200-9.html

Catalyst 9000 Switching – Key Features

Reference

* Limited Availability (LA) only

IOS XE 17.13.1 (Dec'23) SMR	IOS XE 17.14.1 (Apr'24) SMR	IOS XE 17.15.1 (Aug'24) EMR
Enhanced Security ❖ C9400X - GRE over IPSEC with VRF support ❖ SGACL NetFlow drop action record	**Enhanced Security** ❖ C9300X/C9400X - IPSEC Scale enhancements ❖ Secure encryption for IP sftp password *	**Enhanced Security** ❖ 9500X/9600X - MACsec/WAN-MACsec support on Port-Channel Sub-interfaces ❖ AAA PAC-less Authentication ❖ IOSXE SELinux Enforced Mode
Overlays & Segmentation ❖ VXLAN with IPv6 Underlay for Unicast & Multicast ❖ 9500X/9600X - Cisco TrustSec SGT inline tagging	**Overlays & Segmentation**	**Overlays & Segmentation** ❖ BGP EVPN CLI Simplification ❖ Multi-Cluster Fabric – Router MAC Rewrite with NextHop-Self BGP Attribute
Forwarding & Features ❖ BGP feature support on C9200CX ❖ Inter-AS option B MVPN support ❖ IPv6 Proxy Neighbor Discovery	**Forwarding & Features** ❖ PTP Support for C9200CX ❖ IP SLA Probe Config modification via config replace	**Forwarding & Features** ❖ Link Debounce Timer ❖ BGP Router-ID compliance with RFC6286
High Availability	**High Availability** ❖ NAT SSO with StackWise Virtual *	**High Availability** ❖ eXtended Fast Sw Upgrade (xFSU) ≤ 5 seconds - 17.15.2
Platform & Programmability ❖ Map SNMP mibs to YANG xpaths ❖ AAA server MIB Support	**Platform & Programmability** ❖ Energy Consumption Visibility for 9200, 9300 and 9400 ❖ gNMI stream subscriptions with ON_CHANGE mode ❖ AWS S3 and CloudWatch Integration ❖ YANG Model Support for L2NAT	**Platform & Programmability** ❖ Atomic Config Replace (ACR) Phase 1* - 17.15.2 ❖ Enhanced Energy Monitoring ❖ Shutdown Fiber Ports when no SFP Inserted ❖ Shutdown Power Supplies in C9300 StackPower during Low Load
Hardware & Optics ❖ **C9600X-56YL4C** – 56x 50G + 4x 100G Linecard ❖ **C9400-LC-48TX** – 48x 10G Copper (Data-Only) Linecard	**Hardware & Optics** ❖ 1G Support in C9500X/C9600X ❖ New optics support	**Hardware & Optics** ❖ **C9400X-SUP-2/2XL** - 1G support with transceivers

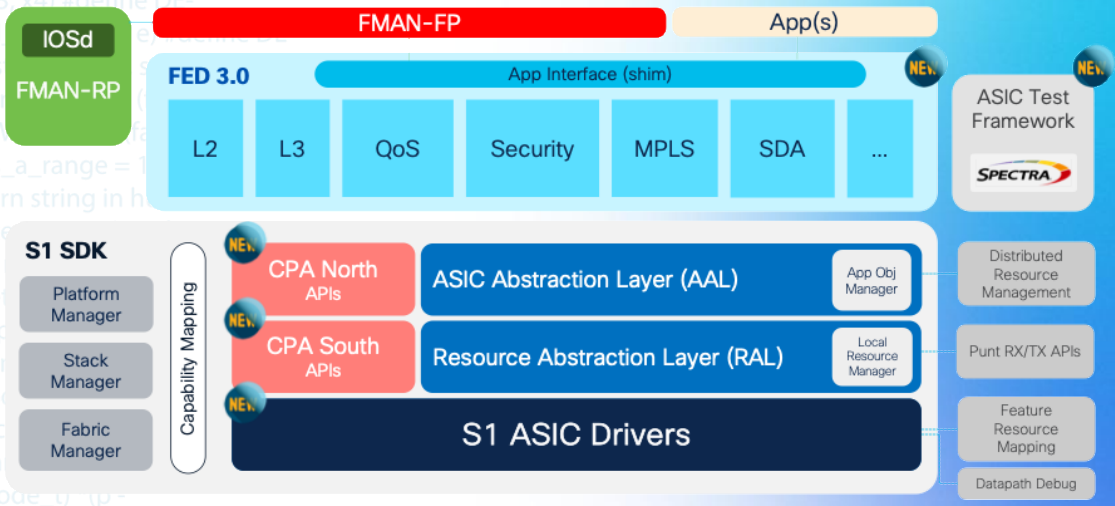


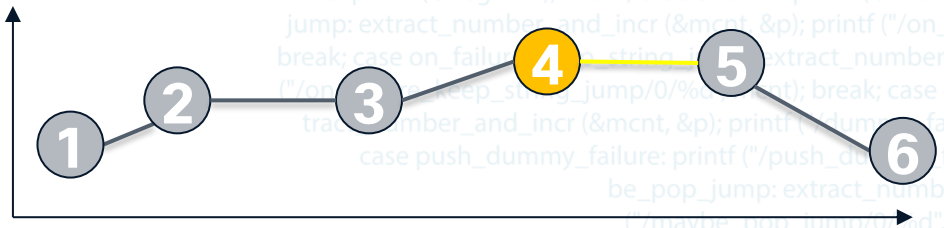
www.cisco.com/c/en/us/support/docs/switches/.../214814-recommended-releases-for-catalyst-9200-9.html

New Cisco 9000 Series

IOS XE 17.16.1 – 17.18.1

Cloud-Native IOS XE





Cisco Catalyst 9000 Switching Portfolio

One Family from Access to Core – Common Hardware & Software

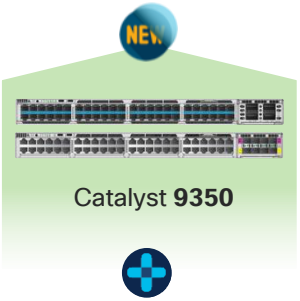
2025+ NEW

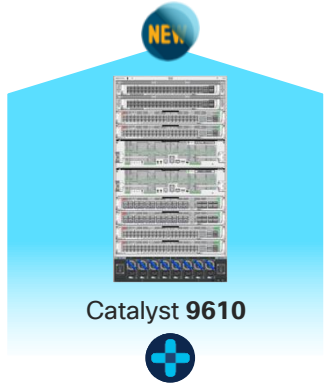
2025 & Later

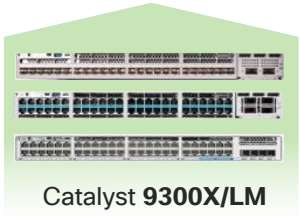
2022 - 2024

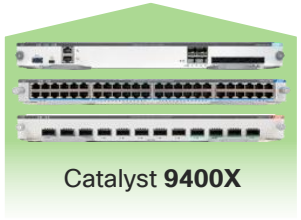
2017 - 2019

2015 & Earlier





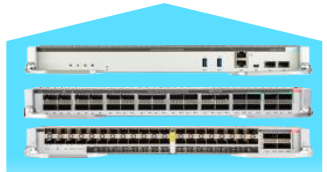




Cisco 9000 series

Cisco IOS XE

Cisco ASICs



Catalyst 2960-X/XR

Catalyst 3650/3850

Catalyst 4500-E Series

Catalyst 3850-XS/4500-X

Catalyst 6840-X/6880-X

Catalyst 6500-E/6807-XL

Access Switching

Core Switching

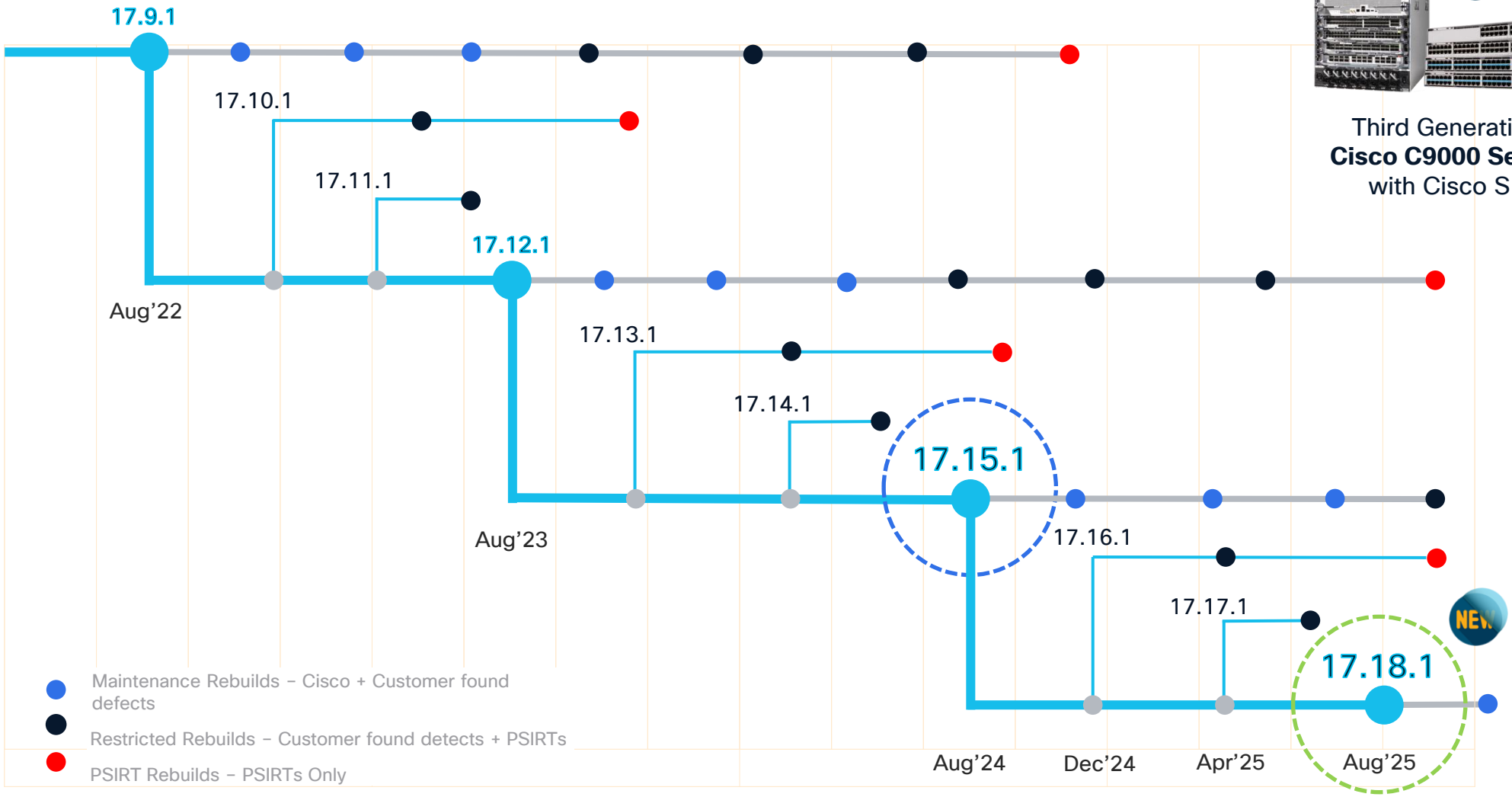
Live!

BRKARC-2092
BRKARC-2098
BRKARC-2099

Cisco IOS XE – Release Schedule

Graphical Overview – 17.16.x to 17.18.x

Third Generation
Cisco C9000 Series
with Cisco S1

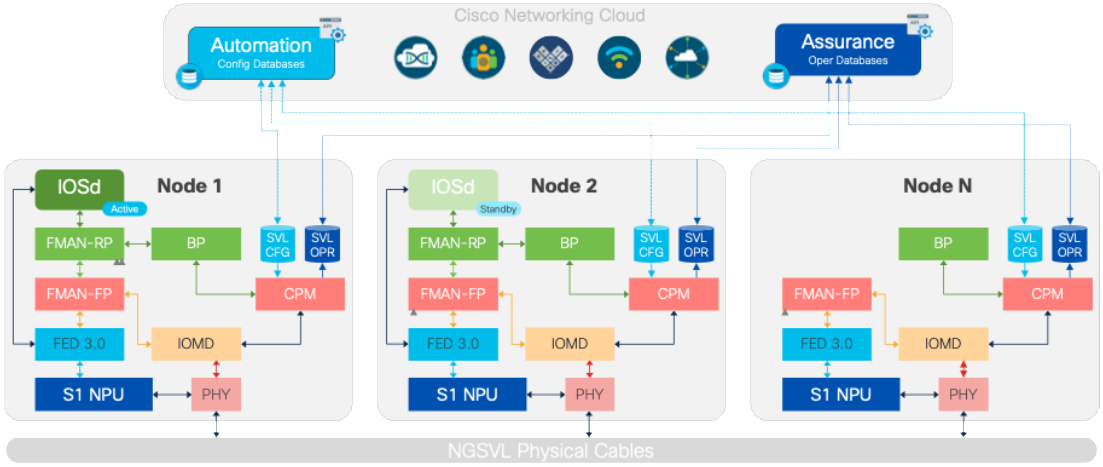


Introducing Cloud-Native IOSXE

Open Cisco IOS XE built for Programmability, Virtualization and AI-Ready

Building a revolutionary NOS architecture with 30 years of experience!

Cloud-Native IOSXE builds on our existing infrastructure abstracting & modularizing internal software processes, with a focus on 'model-driven' objects and standard databases, to enable advanced **programmability**, **clustering** & **resiliency**.



Common Platform Abstraction

Model-driven HW to SW API disaggregation layer (CPA) hides platform hardware details from upper-layers of IOSXE features. Acts as a "single source of truth" for all hardware data.

Model-Driven Hardware & SDK APIs

FED programs hardware and manages the forwarding objects. FED 3.0 is model-driven, ASIC & SDK agnostic, and enhanced for various TDL databases with automatic code generation.

Unified Software & Licensing (UNX)

NEW

Cisco C9K platforms support Unified Management controller models (cloud and/or on-premises) and support a single, common Unified Licensing model.

Cloud-Native Management & AI/ML

NEW

Automation, Assurance & AI-Ops models will support entirely cloud-based, entirely on-premise (e.g. air-gap) or a hybrid of both. Available through a Unified Onboarding.

NG-Stacking & Cluster Infrastructure

NEW

Current StackWise and SVL (protocol & encapsulation) have been redesigned using standard VXLAN based protocols & encap, allowing >8 node ethernet-based (SPF) HA clusters.

Micro-Services Process Modularity

NEW

Modern multi-threaded IOS XE can start/stop individual SW processes on-demand, to enable new services and support real-time SMU and ISSU and enhanced infrastructure HA.

Catalyst 9000 Switching – Key Features

Shipping

* Limited Availability (LA) only

IOS XE 17.16.1 (Dec'24) SMR	IOS XE 17.17.1 (Apr'25) SMR	NEW IOS XE 17.18.1 (Aug'25) EMR
Enhanced Security ❖ CTS: Multiple Static SGTs on interface	**Enhanced Security**	**Enhanced Security** ❖ TWS enhancements (PQC TAM) ❖ SELinux with eBPF ❖ TLS 1.3 for HTTPS, LDAP, RADsec, Syslog, etc.
Overlays & Segmentation ❖ Multi-cluster BGP EVPN VXLAN Fabric : Router MAC rewrite with Next-Hop Self BGP attribute	**Overlays & Segmentation**	**Overlays & Segmentation** ❖ EVPN Multi-Homing (fabric mode) ❖ EVPN Policy-Based Routing (PBR) with Next-Hop Self ❖ LISP EID-level Pub-Sub ❖ Security Service Insertion (SSI) ❖ Multicast VPN (mVPN) on C9500X, C9600X-SUP-2
Forwarding & Features ❖ Multicast Flow-Aware SG-timer ❖ ECMP support with NAT Scale ❖ STP bridge assurance per-interface	**Forwarding & Features**	**Forwarding & Features** ❖ L2, L3, Multicast for C9350 & C9610 ❖ ACLs, QoS & FNF for C9350 & C9610* ❖ Inter-AS Option B on C9500X, C9600X-SUP-2
High Availability ❖ Quad-Sup StackWise Virtual on 9600X-SUP-2 ❖ Enhanced XFSU for 9300/9300X (≤ 5 sec)	**High Availability** ❖ Uplink Sequencing with C9400	**High Availability** ❖ SSO for C9350 Stacking, C9610-SUP-3 ❖ NG-Stackwise for C9350 & C9610*
Platform & Programmability ❖ C9200CX ZTP: External Connectivity ❖ FQDN Enhancements ❖ Auto-off switchport LED C9200, C9300 ❖ Auto-off C9200, C9300 Fiber Ports when no SFP Inserted ❖ Auto-off C9300 Power Supplies in StackPower during Low Load	**Platform & Programmability** ❖ LLDP support on C9300L management port for Zero-Touch Provisioning (ZTP) ❖ C9400: 2100AC Titanium PSU Support	**Platform & Programmability** ❖ Meraki Dashboard for C9200/L, C9500 ❖ Unified Management for C9350 & C9610* ❖ Unified Licensing for C9350 & C9610* ❖ Unified Onboarding (Native TLS) ❖ Enhanced Energy Monitoring – Smart Power ❖ Atomic Config Replace (ACR) Phase 1 – GA ❖ OpenConfig support for L2/L3, Multicast & EVPN
Hardware & Optics ❖ QSFP-100G-FR-S support on C9400X-SUP-2/XL	**Hardware & Optics** ❖ QSFP-100G-LR4-S support on C9400X-SUP-2/XL ❖ QSFP-100G-LR4-S support on C9600-LC-40YL4CD & LC-32CD	**Hardware & Optics** ❖ **Cisco C9350 Series** – Phase 1 ❖ **Cisco C9610 Series** – SUP-3/XL, Native LCs, LC-ADPT

cisco

High Availability (SSO)

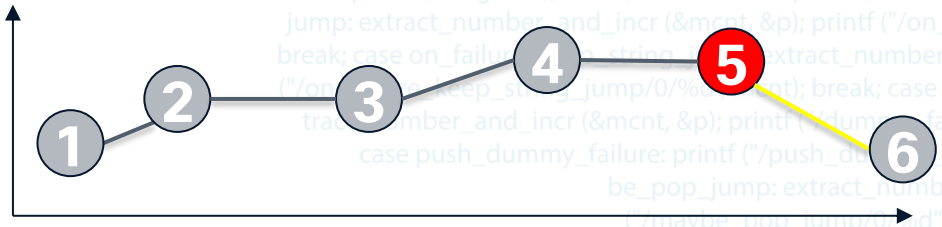
ISSU & xFSU

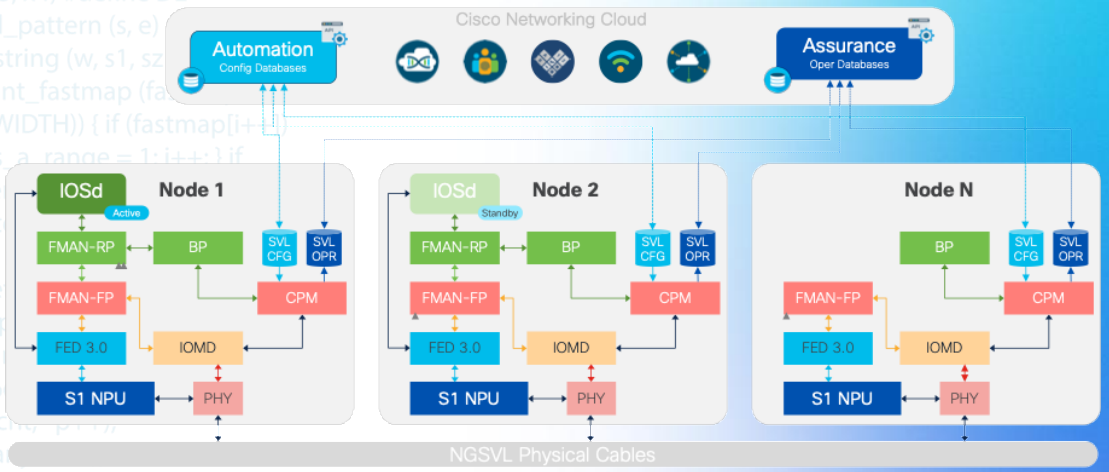
NG Stackwise

Programmability

Model-Driven

Application Hosting





Campus Switching Innovations for Future Proofed Workspaces

BRKENS-2609

Campus Switching Innovations for Future Proofed Workspaces

Minhaj Uddin- Leader Technical Marketing, Cisco

Modern workspaces demand secure, scalable, and high-performing networks to support hybrid work, IoT, next-gen technologies, and sustainability goals.

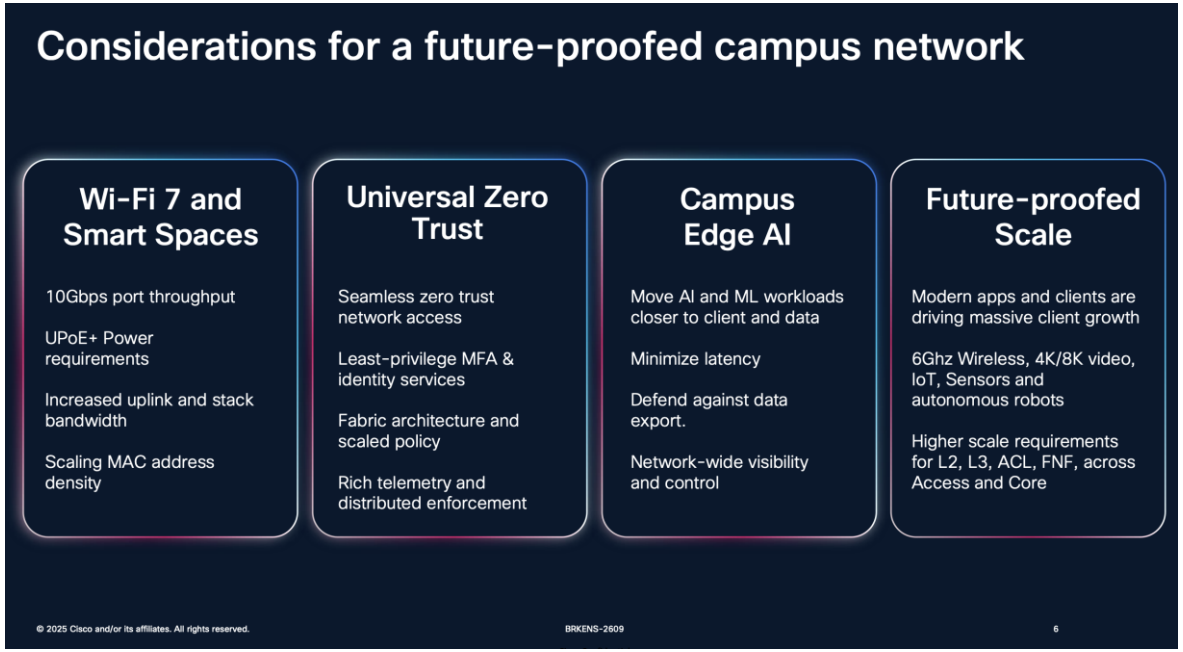
This session introduces **Cisco's new switches** alongside **key innovations**, such as pervasive security, AI-driven insights, software-defined access, and cloud management.

Discover how these solutions simplify management, enhance scalability, boost energy efficiency, and enable smart, resilient, and sustainable environments ready to meet tomorrow's challenges.

CiscoLive Melbourne 2025

Room 217, 1:00-2:30 PM, Wednesday 12th

www.ciscolive.com/apjc/learn/session-catalog.html?search=BRKENS-2609



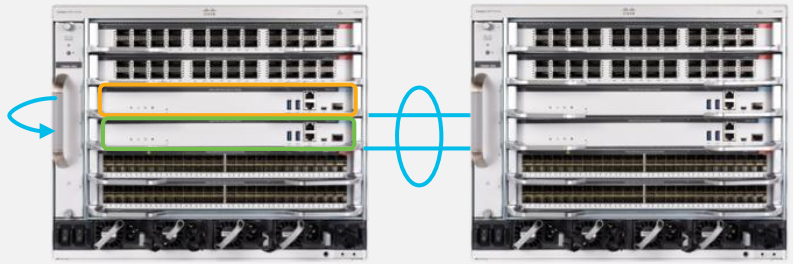
Mission-Critical Resiliency

Your business stops if the network is down

Cost of only **one hour** of downtime to an average enterprise **> $300,000****

*** Based on industry reports from Gartner and ITIC*

Catalyst 9600 Series
(Dual chassis w/ StackWise Virtual)



Catalyst 9400 Series

Catalyst 9500 Series

Architecture

StackWise® + StackWise Virtual

- Virtualized redundant systems for simplified configuration & protocols

Graceful Insertion/Removal (GIR)

- No downtime when device in maintenance mode

Operating System

Software Maintenance Upgrade (SMU)

- Minimal or no downtime patches

In-Service Software Upgrade (ISSU)

- Upgrade with minimal or no traffic loss

Extended Fast Software Upgrade (xFSU)

- < 5 sec downtime - Stack upgrade

Platform

Redundant Supervisors

- Modular with SSO/NSF
- SVL Quad-SUP RPR

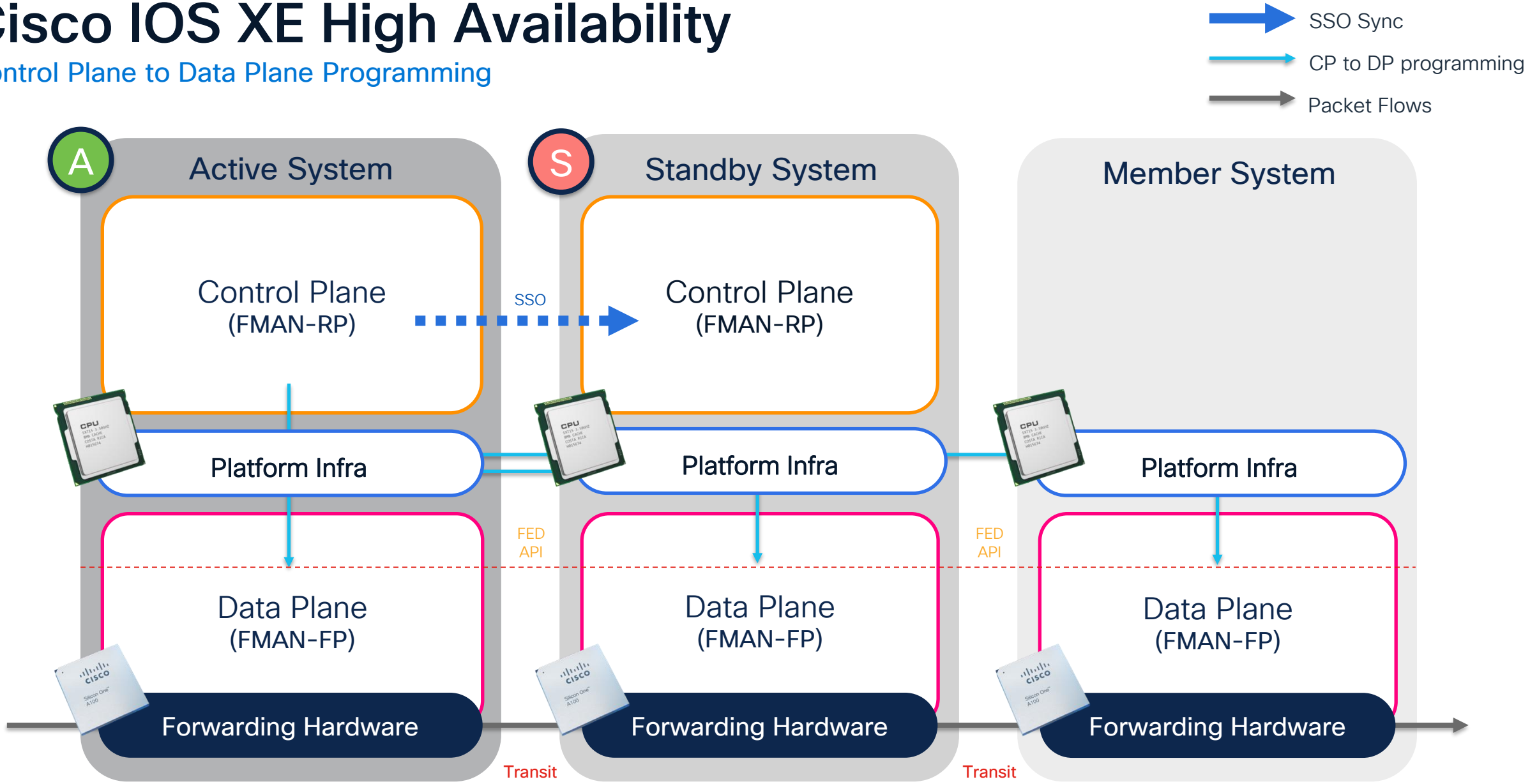
Redundant Power & Fans

- In case of any hardware failure

Eliminate downtime with ***High Availability*** designed at every level

Cisco IOS XE High Availability

Control Plane to Data Plane Programming



IOS XE Install – SMU patches

Patch a previously ‘certified’ image, without full upgrade

DNAC Version: Guardian 2.3.3
License Level : DNA Advantage

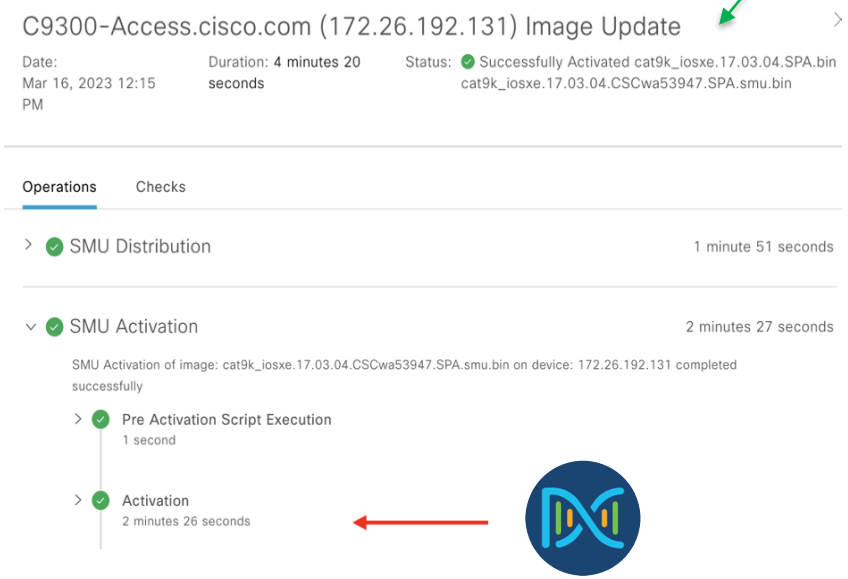
Software Maintenance Update (SMU) is a small **software package** that can be installed for a **fix** or **security resolution** on a released version.

- **Hot Patching** – does not require explicit reload after installation to get activated. (not traffic-affecting)
- **Cold Patching** – requires a system reload after installation to get activated. (traffic-affecting). The 9200 family supports only this.

NEW

- **Bundle SMU** – One single SMU file containing and applying multiple SMU fixes at once.
- **Independent SMU** – One single SMU file tailored to address a specific bug or vulnerability.

Patching can also be performed using Cisco Catalyst Center



Reduces both time and scope for [re]certification

Self-sufficient and reliant bug fix solution for PSIRT, CFD & IFD

Hitless Zero-Downtime with Hot Patching

EMR Releases with 371 SMU files available

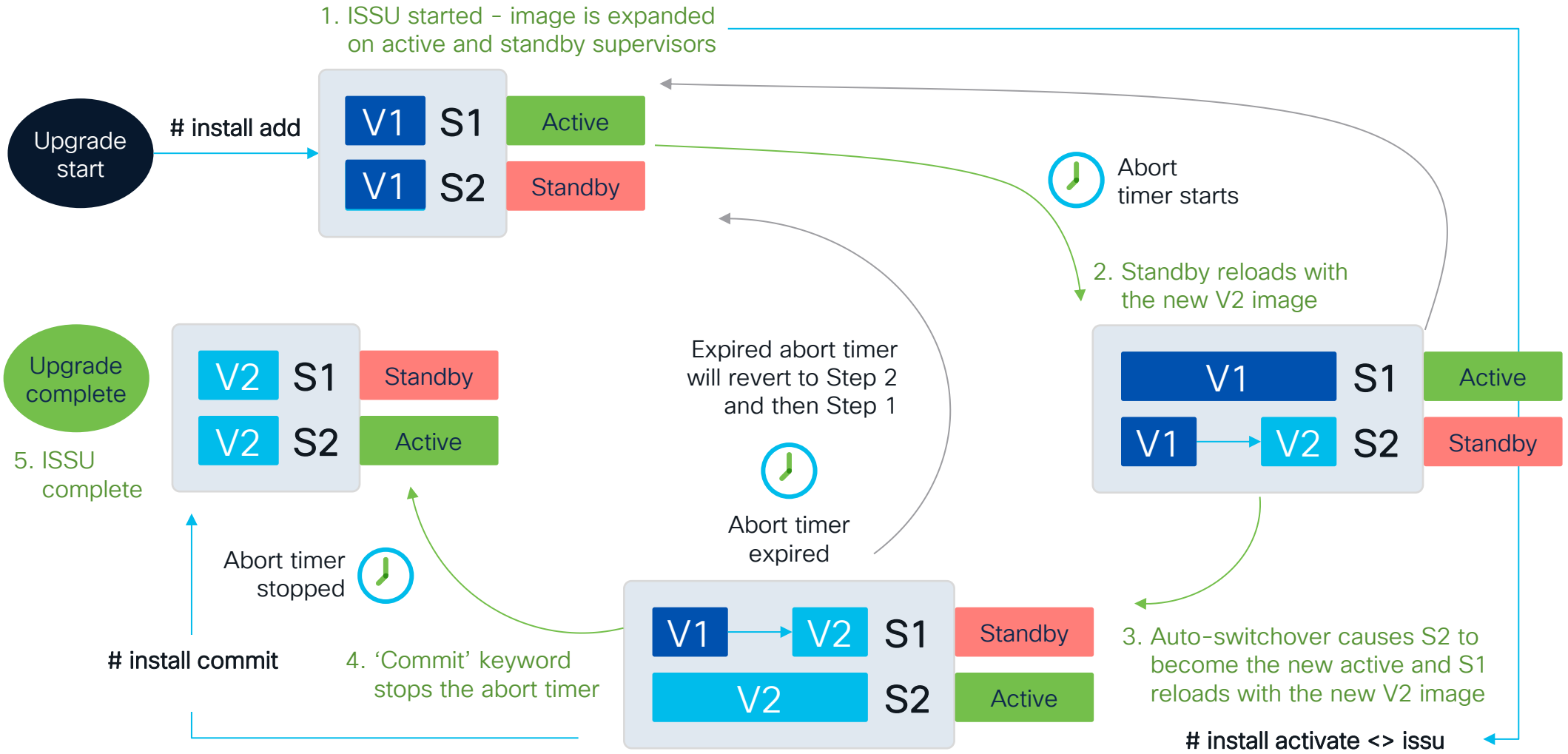
LAN High Availability

In-Service Software Upgrade (ISSU)

Catalyst 9600/X

Catalyst 9500/X

Catalyst 9400/X



If S2 fails to become the active, it will revert back to Step 1

LAN High Availability

Extended Fast Software Upgrade (xFSU)

NEW. ≤ 5 Seconds - 17.15.2

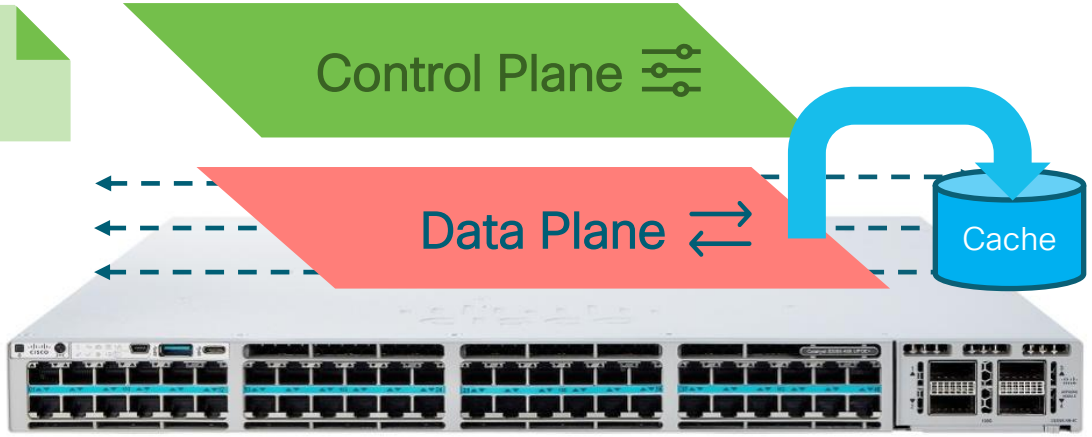
C9300X (≤ 30s) - 17.7.1

C9300/L (≤ 30s) - 17.3.2

Command to trigger xFSU

C9300# ***install add file*** *<image>* ***activate xfsu commit***

Control Plane Upgrade
V1 ⟶ V2



Data Plane upgrade
V1 ⟶ V2

C9300 | C9300L | C9300X

Cisco xFSU minimizes downtime to less than 5 seconds (standalone or stack)

Cisco IOS XE Programmability

Full Telemetry “Stack”

DEVNET

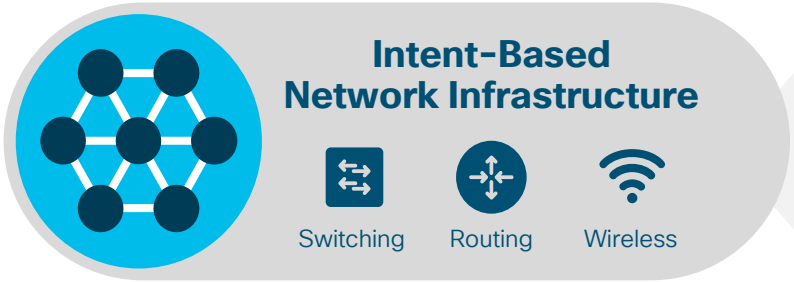
developer.cisco.com/site/IOS XE

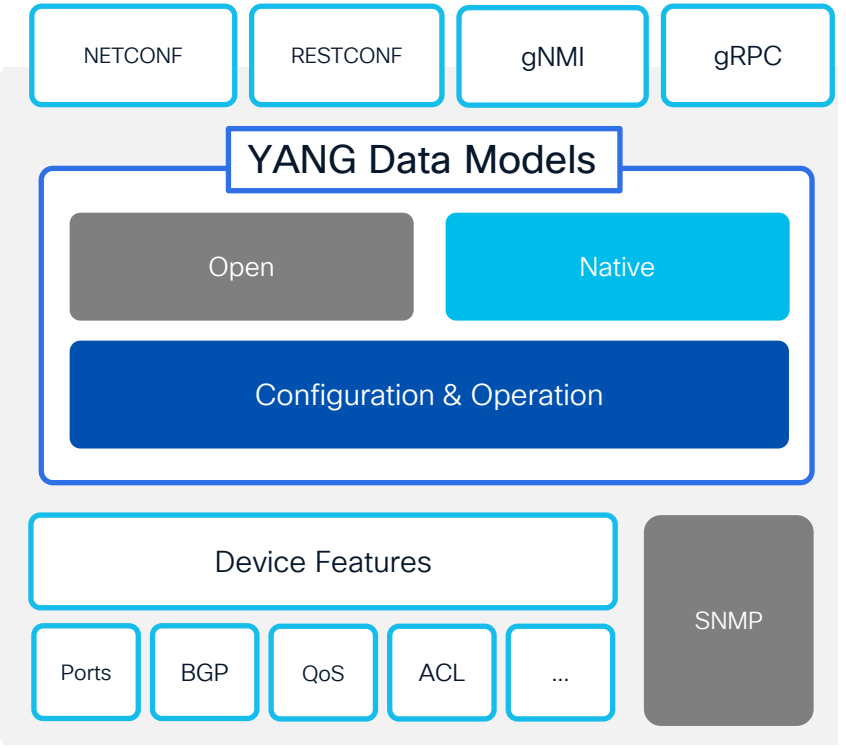
CLI

WebUI

NETCONF, RETCONF, gNMI & gRPC are programmatic interfaces that provide additional methods for interfacing with an IOS XE device

YANG data models define what is available for configuration and operational telemetry





IETF

OpenConfig

IEEE

cisco

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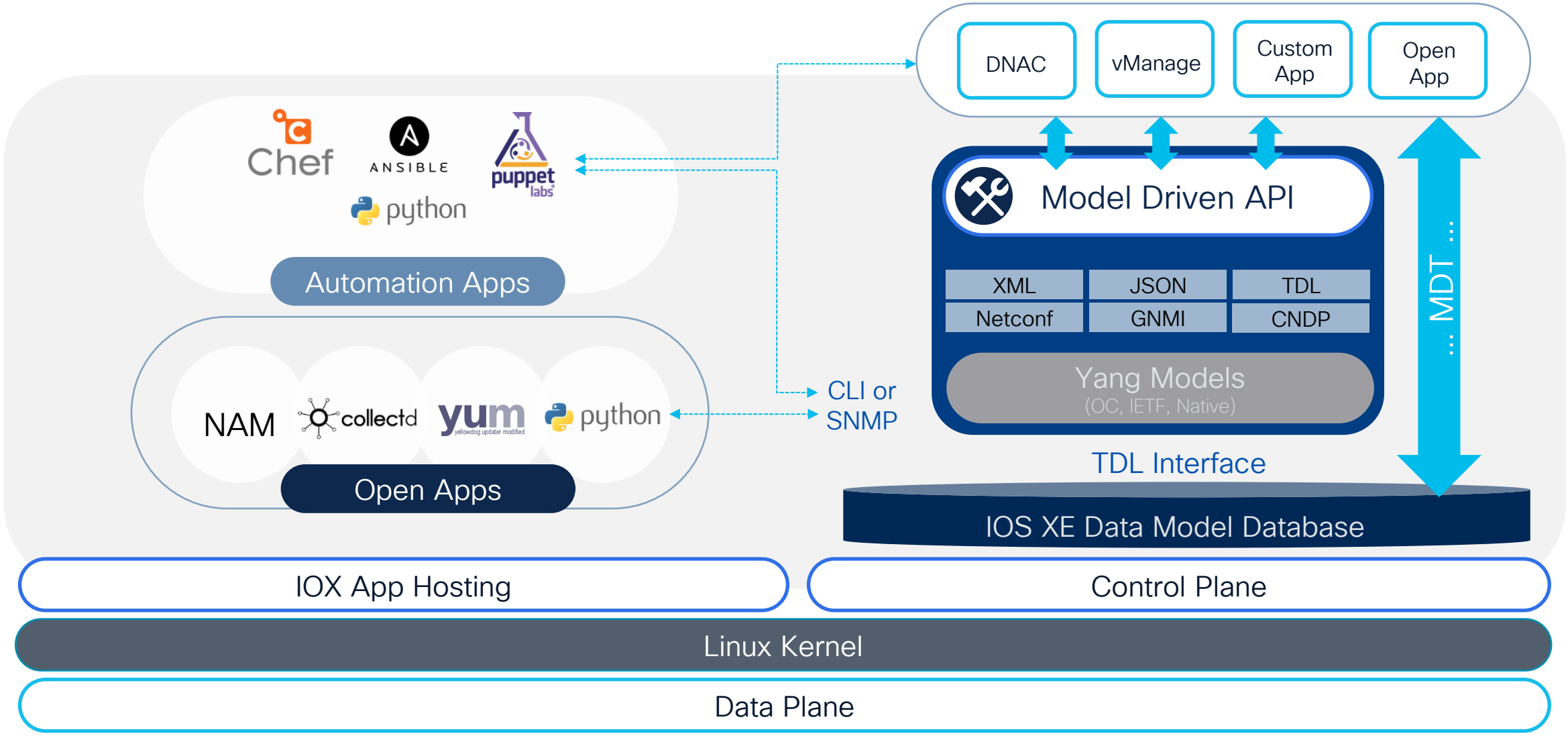
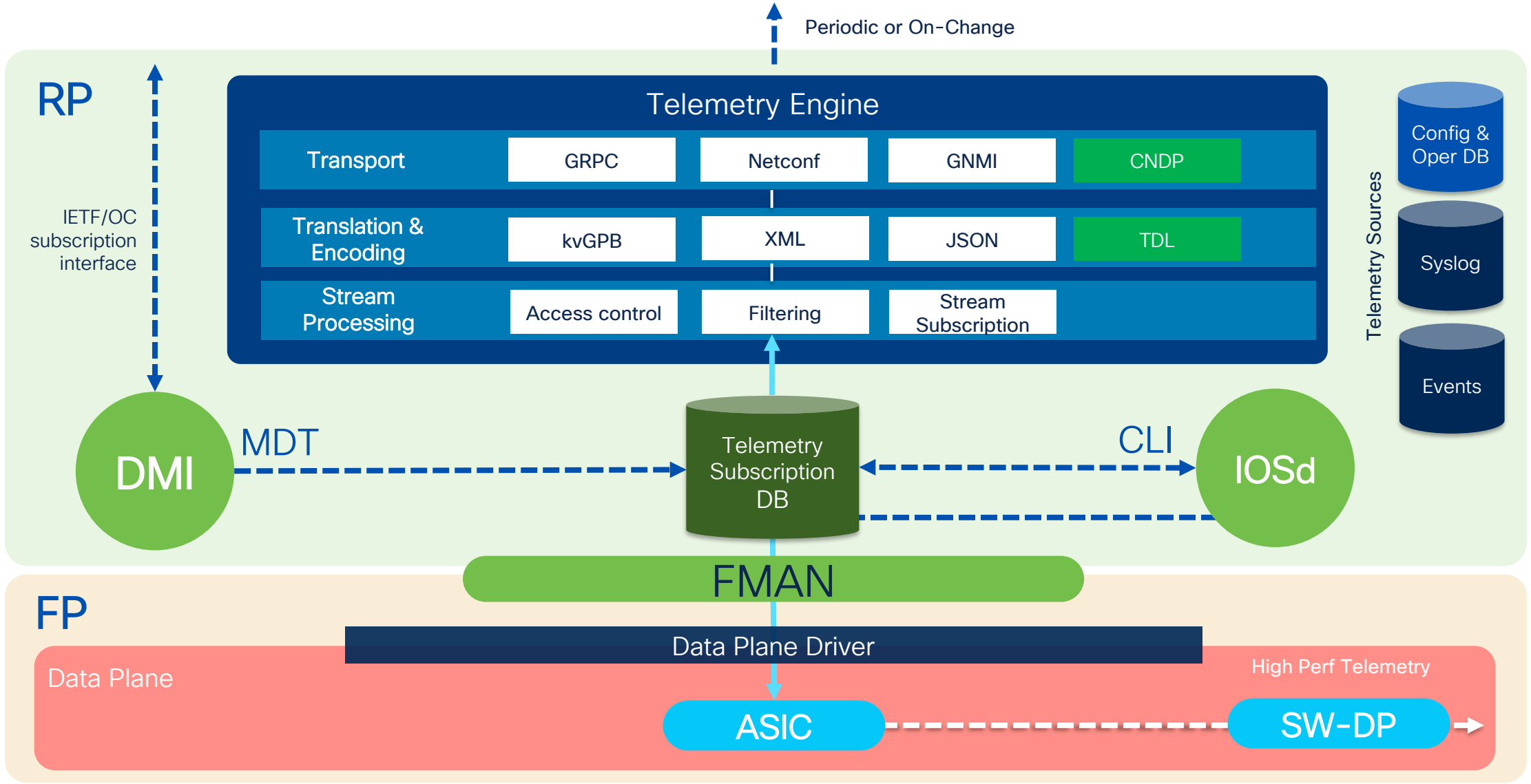
Cisco IOS XE – Management

Management Plane – High-Level Overview



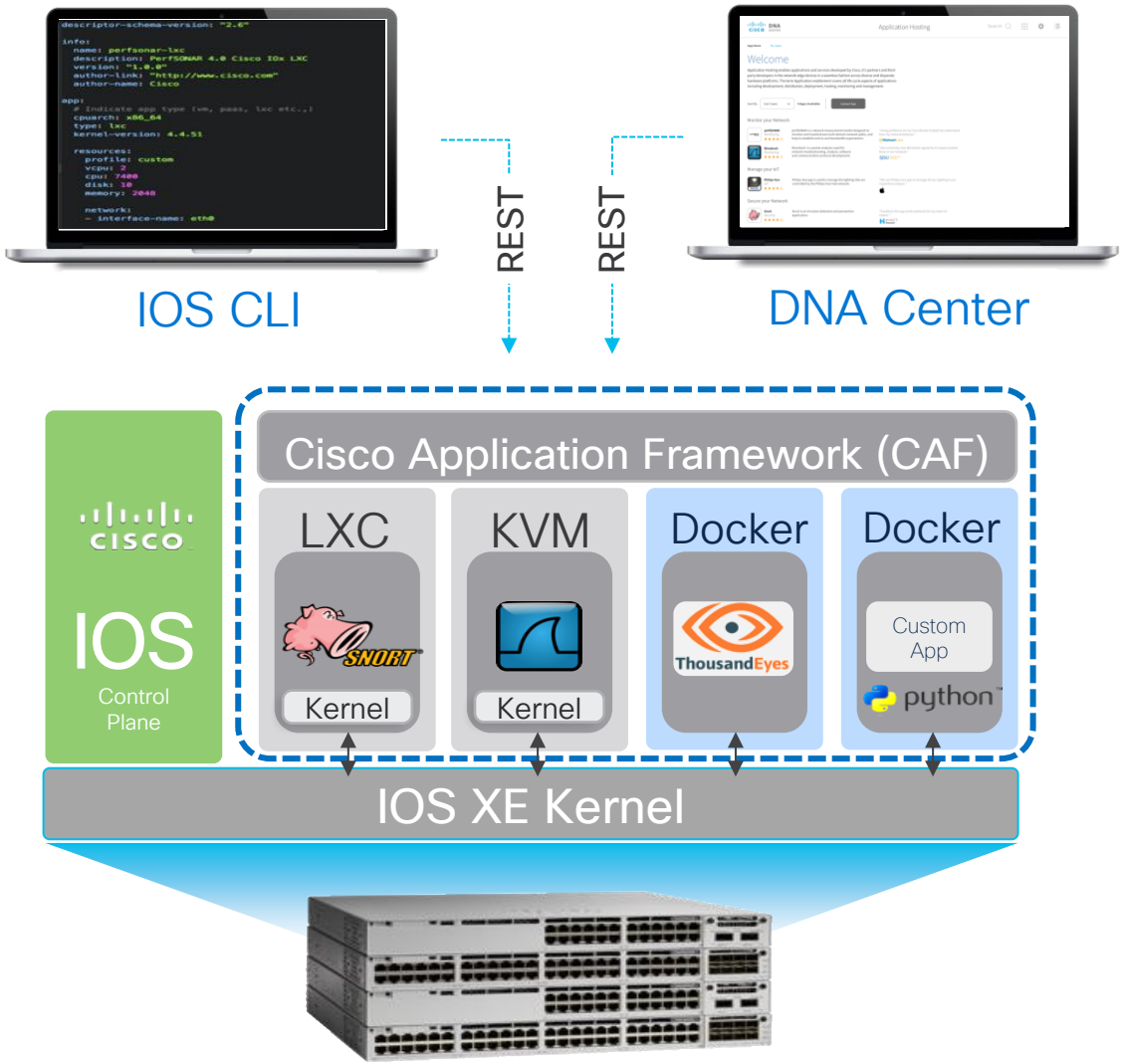
Cisco IOS XE - Model-Driven Telemetry

MDT Architecture



Cisco IOS XE

Application Hosting



TRex Realistic Traffic Generator · Attivo Networks · Hawkeye

TRAFip · ThousandEyes · NETBEEZ

perfSONAR · Snort · AWS Greengrass

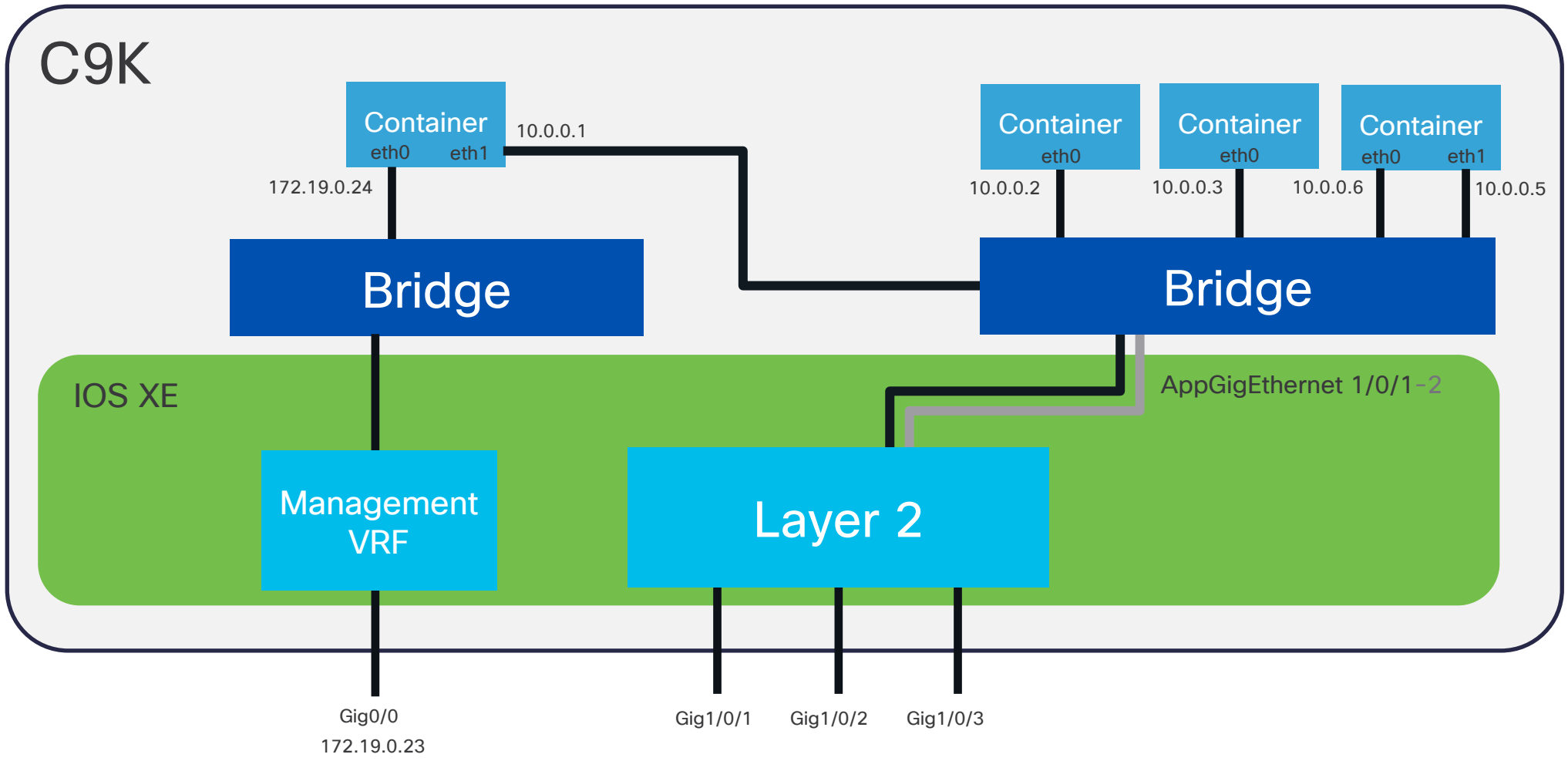
ISC DHCP Server · BIND 9 · iPerf

Nagios · Alleantia · More...

- Cisco will not support third-party apps or open-source apps, unless specifically called out
- Such apps, however, will be validated for compatibility on Catalyst 9000 switches
- DevNet ecosystem will indicate the partners who have worked on Catalyst 9000 switches

Catalyst 9000 Series – App Hosting

Container Networking



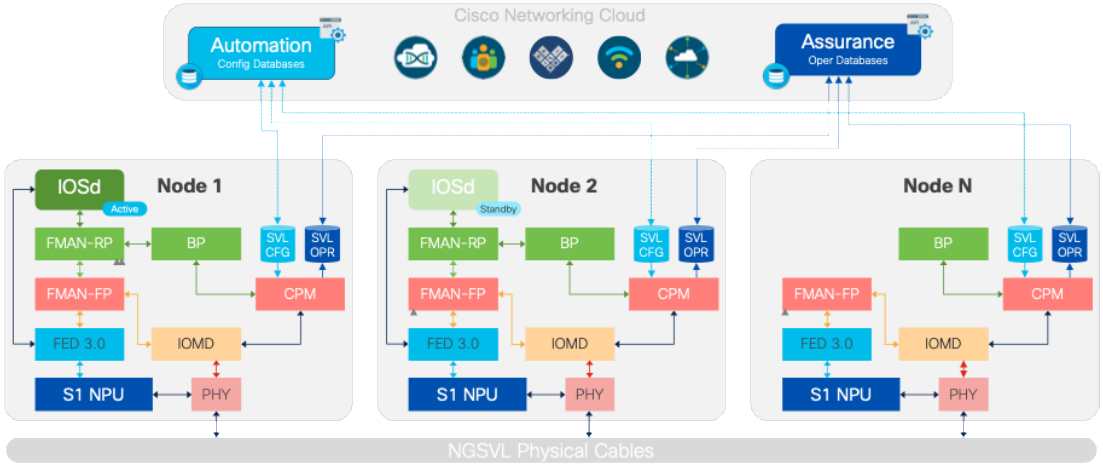
Introducing Next Generation Stackwise

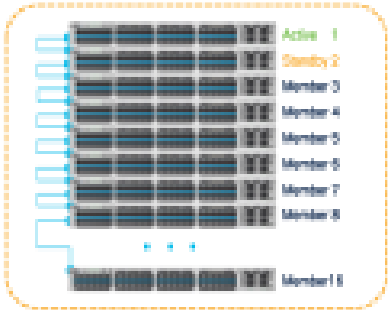
A new era of micro-services device clustering

A new Stacking Architecture

based on standard Ethernet protocols!

Cloud-Native IOSXE includes a **new Stack architecture** based on standard Ethernet protocols and encapsulation. Using either back-side or front-side ethernet links - for **greater scale**, **stability**, better **SSO convergence**, and **ISSU/XFSU** & **SMU** for hitless software upgrades.





How is the Architecture new?

- A new Bootstrap Process (BP) & Cluster Process Manager (CPM), as a separate Linux thread.
- Runs IP SPF + VXLAN-GPO over standard Ethernet

Is it front panel or back panel?

- Both! Dedicated cables or Transceivers + cables.
- Stack Interface (SIF) is treated as any ethernet port

Can I still manage it the same?

- Familiar (same) config and show commands
- Uses same '*stackwise*' & '*stackwise-virtual*' CLI

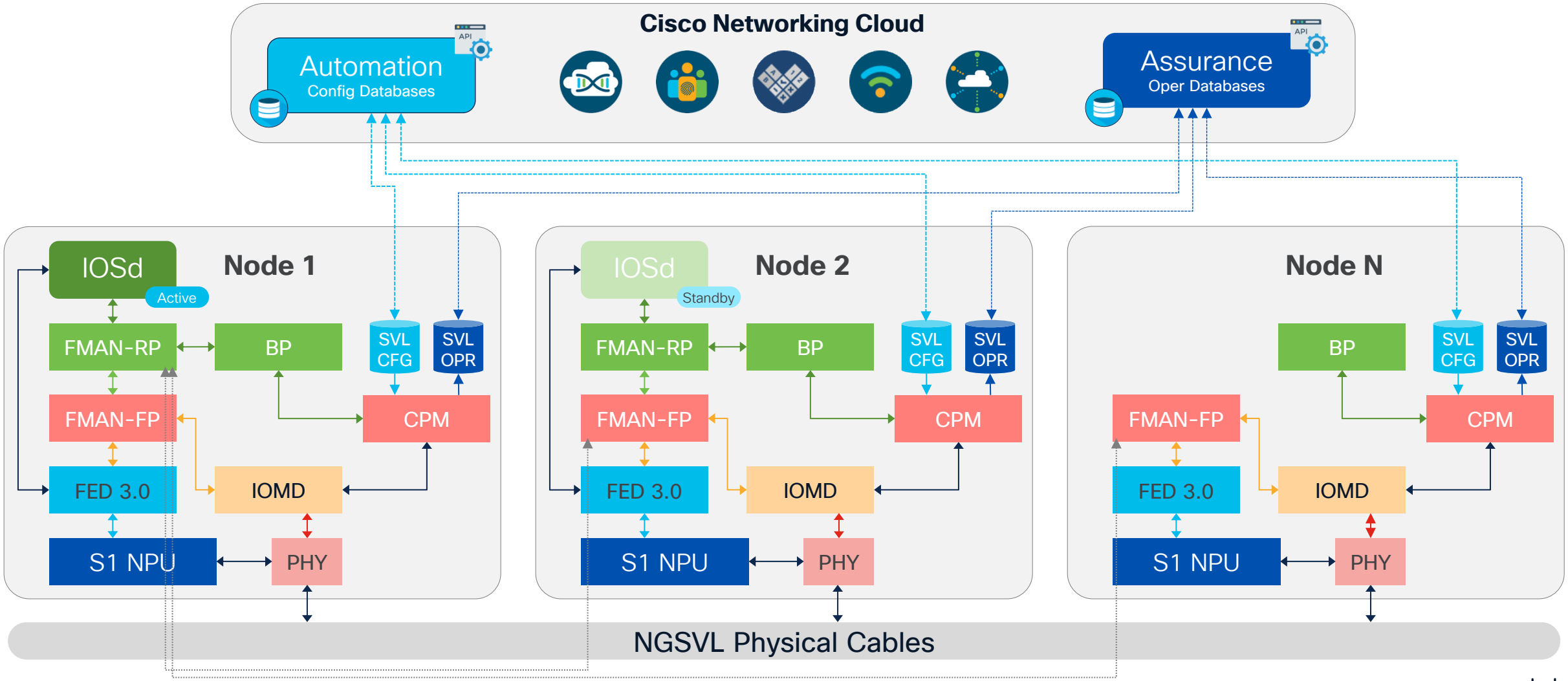
How does it benefit me?

- Common to both C9350 & C9610
- Simplified cabling & dynamic link add/change
- Improved SSO and ISSU/SMU convergence

... and much more, coming soon

What is Next Gen Stackwise?

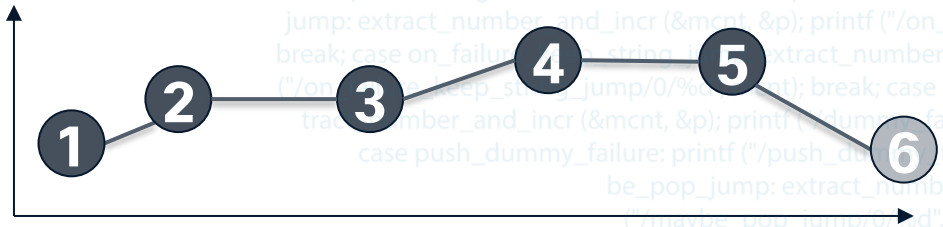
Introducing an entirely new Stacking Architecture

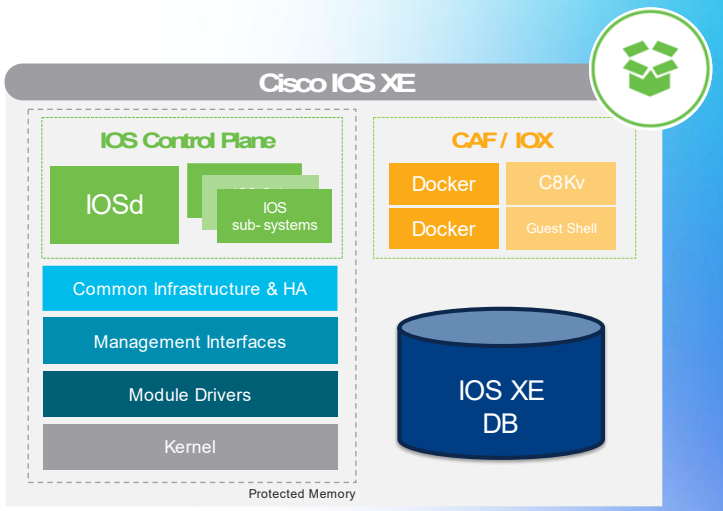


NOTE: Simplified Diagram

Glimpse into the Future

Software Innovations for Enterprise Switching





Making Cisco C9000 Series into Campus “Smart Switches”

Enhanced Control-Plane and AI-ready App-Hosting

x86

Cisco C9000 Series Switches have supported **Application Hosting** & **Edge Computing** for years!

We are bringing these capabilities to a new level with **more Apps**, **Multi-App** hosting and hardware-support for **Edge AI/ML agents** or **Hypershield agents**

C9350

C9350 Standard SKUs

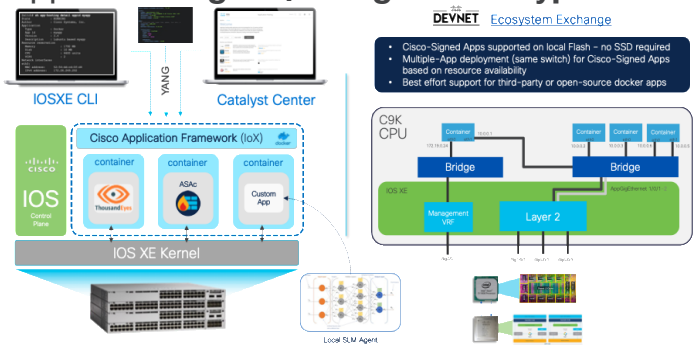
- **Class:** Low/Med CPU
- **Intel** Gen12 RPL Core i3
  - **4E+2P-Core** (2.5 GHz)
  - **16GB DDR5** (4800 MHz)
  - **4x 10G NIC*** (X710)
  - **USB3.0 SSD** (External)

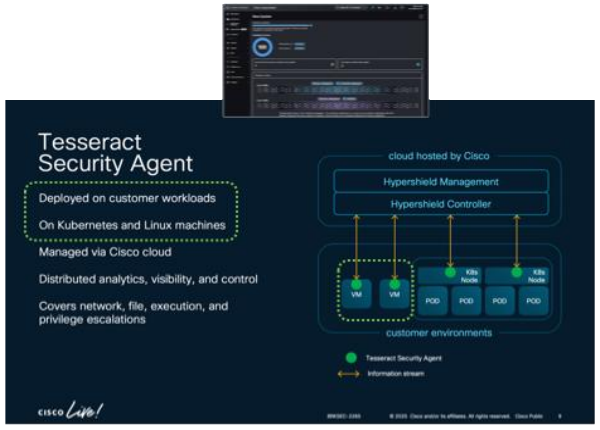
* Hardware-capability. 2x AppGig for FCS

C9610-SUP-3/XL

C9610-SUP-3/XL SKUs

- **Class**: Med/High CPU
- **Intel** Gen10 ICX Xeon D
  - **8P-Core** (2.0GHz)
  - **32GB DDR4** (2400 MHz)
  - **4x 25G KR***
  - **M2 SATA SSD** (External)





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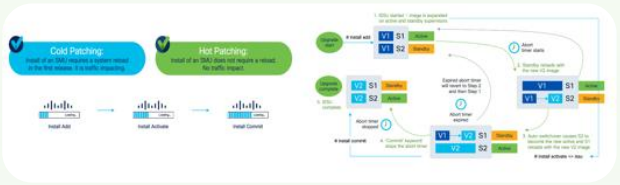
Where are things going?

Features & Scale

More details in PPT Notes

SMU & XFSU/ISSU



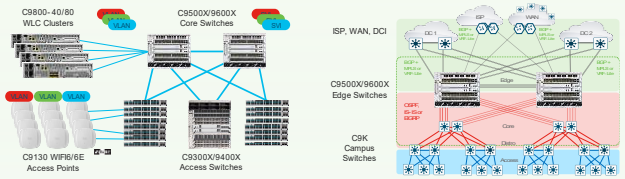
Patch an existing (certified) IOS XE version

- Bug fixes and new (rebuild) features
- Critical software vulnerabilities (PSIRT)

Sub-second In-Service Software Upgrades

- Redundant Supervisors and SVL
- Standalone (xFSU) and Stackwise

MAC & IPv4/v6 Scale



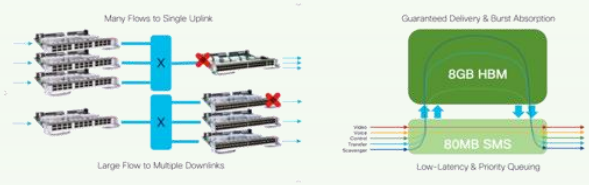
Increasing MAC scale for Wireless & IOT

- WLC to Core SVI scale growing ≥256K MACs
- WIFI6E, 5G and IOT Devices & Sensors

Increasing IPv4/v6 scale for Internet & VPN

- Collapsed LAN Core + SP/WAN Edge designs
- IPv4 GRT is ≥850K and IPv6 GRT is ≥50K

VoQ & HBM



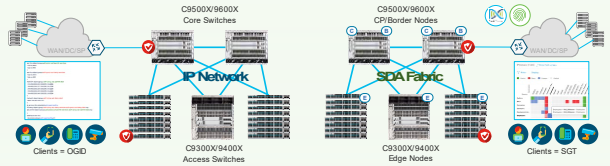
Virtual Output Queues (VoQ) for high throughput

- Eliminate Head-of-Line Blocking at egress
- Support for logical (e.g. sub) interfaces with HQoS

Local and Expandable HBM for optimal buffering

- Local buffers for low-latency strict-priority queuing

OGACL & SGACL



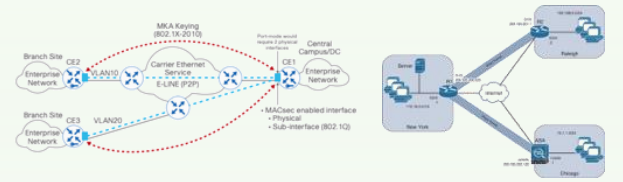
Object-Groups map IP/mask to Labels in CEM

- User defines IP/masks to simple OG/SG name
- OGID/SGT labels are stored in Exact Match table

OG/SGACL ACEs take minimal space in TCAM

- Only the Permit/Deny ACEs stored in TCAM
- OG/SGACL with same ACEs can reuse entries

WAN MACsec & IPsec



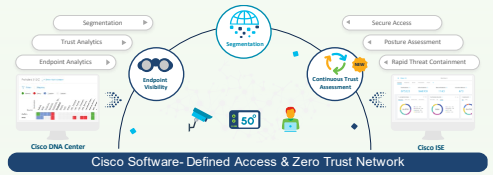
256-bit Hardware Encryption over L2

- P2P LAN MACsec with 802.1ae
- P2MP WAN MACsec with 802.1q ClearTag

256-bit Hardware Encryption over L3

- P2P SVTI IPsec with IKEv2, ESP
- Supports Site-to-Cloud (AWS, Azure, Zscaler)

SDA & ZTNA



SD-Access Fabric with Group-Based Policy

- L2/L3 virtual overlay, with macro & micro segments
- Full automation, assurance & policy with Cisco DNA

Application & Endpoint Identification & Analytics

- Hardware Flexible NetFlow and IPFIX
- AVC/NBAR2 and SDAVC/CBAR to ID clients & apps

Summary

Catalyst 9000 with Programmable ASICs

Benefits for your network

- ✔ **FLEXIBILITY** and
- ✔ **ADOPTABILITY**

Enabling **Network Evolution**
on your journey to
AI-Ready Secure Networking

Catalyst 9000 with Cisco IOS XE

Benefits for your network

One Release Train

Operational Efficiency,
Consistency in Behavior,

Common Features

Feature Velocity
across Platforms

Updates & Patching

Sub-package upgrades,
Cold and Hot Patching

Native Programmability

Object based model,
Netconf/REST Interfaces

Trustworthy & Secure

64-bit ASLR, Secure Boot,
Hardware TAM

Catalyst Leadership in Enterprise Networks

New Feature
Enhanced

A Platform based Approach

Catalyst Center and Meraki Dashboard

32M Network Devices Managed

19M APs | 6M Switches | 2.5M Routers | 830M Clients

17M
Devices on Catalyst Center

15.3M
Devices on Meraki Dashboard

Cisco C9000 Family

100,000+ Customers, Millions of Switches

"Catalyst 9K continues to be the fastest ramping product in the company's history"

Secure Networking

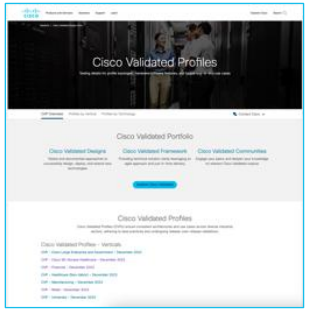
- Common Policy
- Secure Equipment Access
- SD-Access (LISP & EVPN)
- High-speed Encryption

Digital Experience

- Campus Automation
- AI Endpoint Analytics
- ThousandEyes Digital Experience
- AI Ops & Assurance

Operational Simplicity

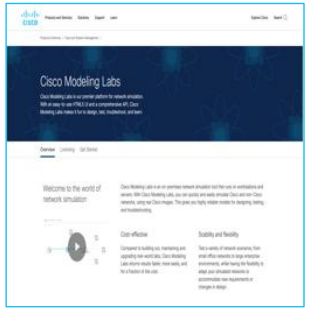
- Cloud Managed Catalyst
- Infrastructure as a Code
- S3 & CloudWatch Integration
- Visibility, Control & Rollback



Cisco Validated Profiles (CVP)

Industry Validated Reports

Industry Certifications



Cisco Modeling Labs

BRKARC-2092

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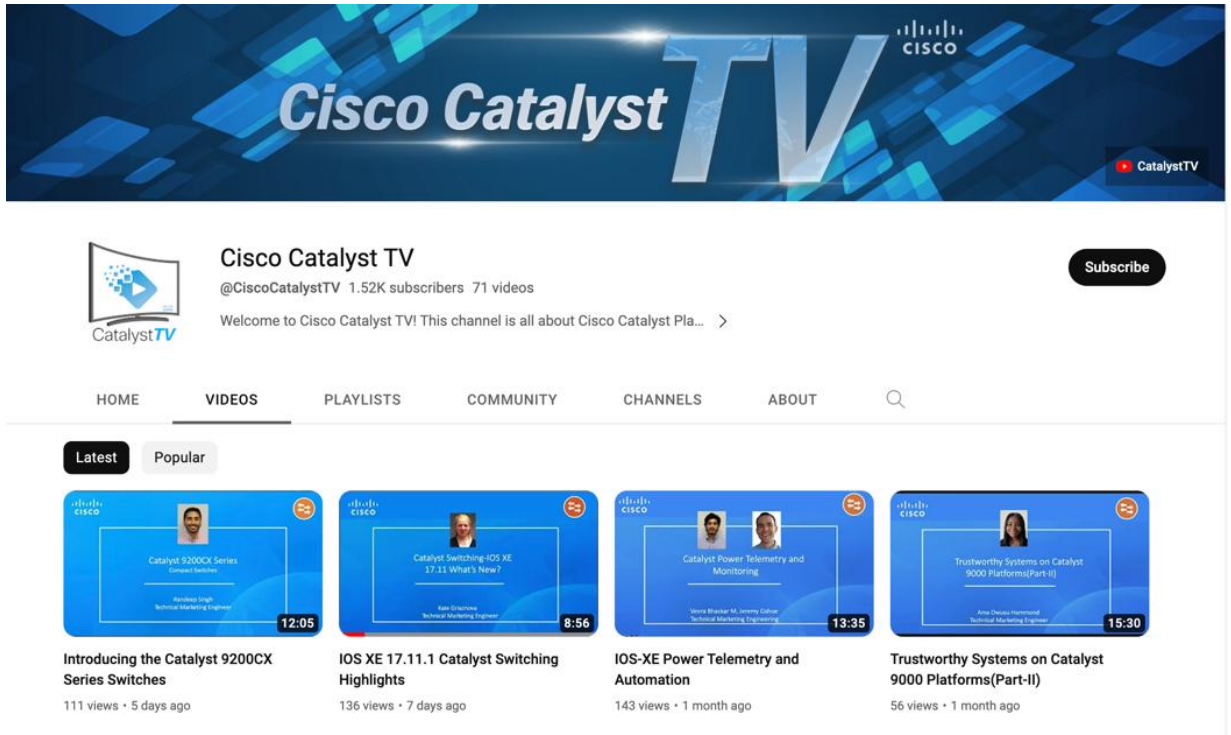
Catalyst 9000 Switching - Useful Resources



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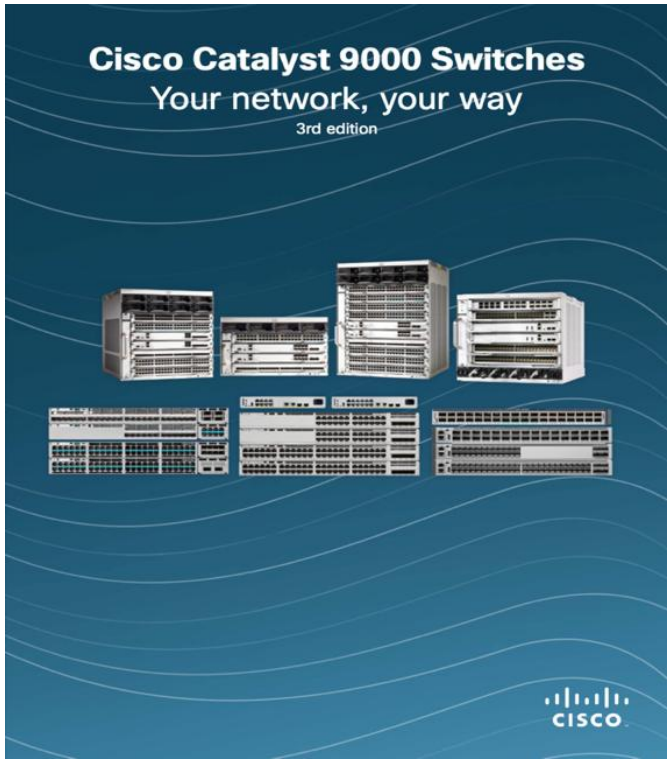

cs.co/cat9kbook

Cisco Catalyst 9000 switches - Your Network, Your Way (3rd Edition)
Cisco SD-Access for Industry Verticals - From Design to Migration

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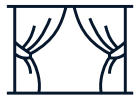

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