What's new in Cisco Smart Stacking on Cisco C9K?

Cisco 9350 & C9610 Series Campus Switches

Shawn Wargo
Principal TME

#HighBitRate

Webex App

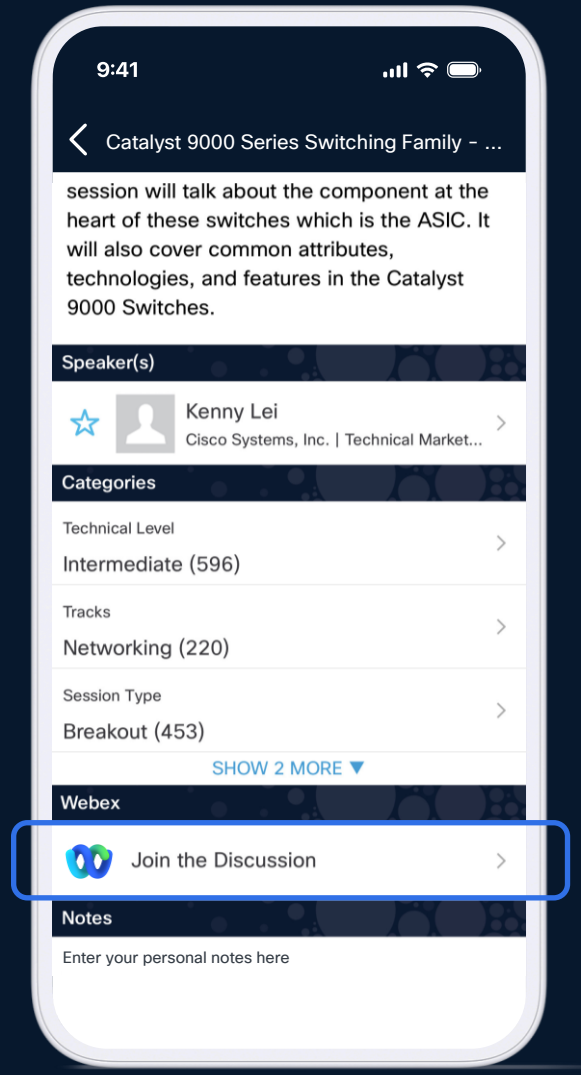
Questions?

Use Webex App to chat with the speaker after the session

How

1. Find this session in the Cisco Events App: **BRKENS-2504**
2. Click “Join the Discussion”
3. Install the Webex App or go directly to the Webex space
4. Enter messages/questions in the Webex space

Webex spaces will be moderated by the speaker until February 27, 2026.



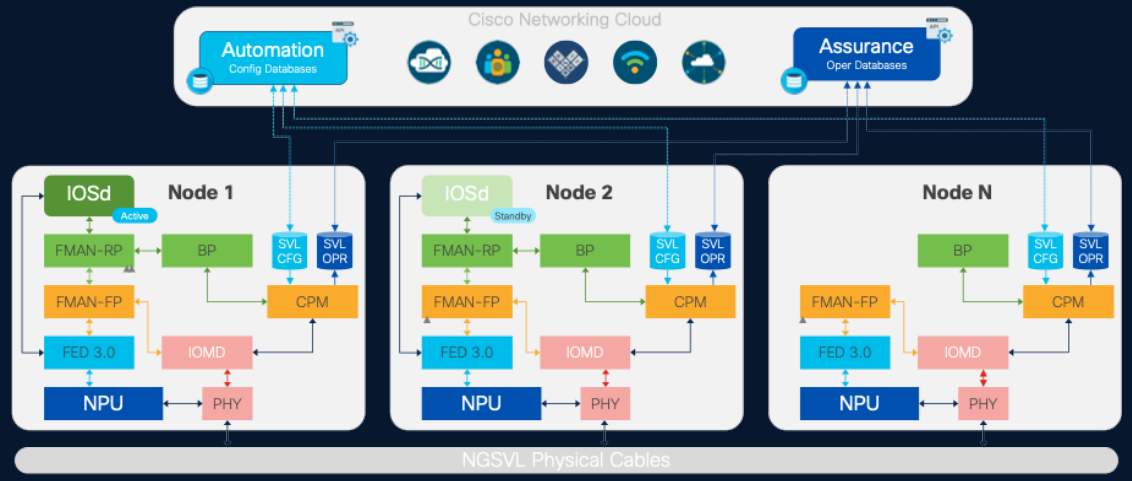
Introducing Smart Stacking (NG-SVL)

A new era of micro-services network device clustering

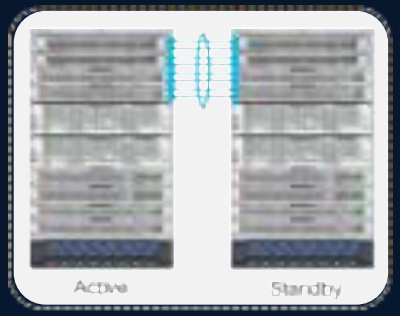
NEW

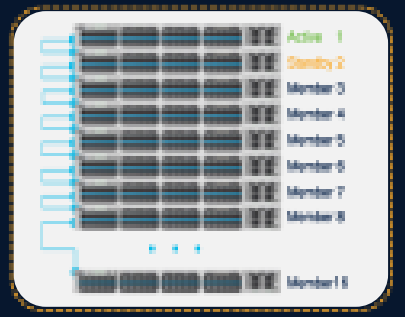
A new Stacking Architecture
based on standard ethernet protocols!

Cloud-Native IOSXE includes a new Stacking architecture based on standard **ethernet protocols** and **encapsulation**. Using either back-side or front-side ethernet ports for greater **scale**, enhanced **stability**, faster **SSO convergence**, and better **ISSU/XFSU** & **SMU** for hitless software upgrades.



C9610





C9350

How is the Architecture new?
- A new Bootstrap Process (BP) & Cluster Process Manager (CPM) - as a separate Linux thread
- Runs ISIS SPF + VXLAN-GPE on standard Ethernet

Is it front panel or back panel?
- Either! Dedicated cables or Transceivers + cables
- Stack Interface (SIF) is treated as an ethernet port

Can I still manage it the same?
- Familiar (same) config and show commands!
- Uses "*stackwise*" or "*stackwise-virtual*" CLIs

How does it benefit me?
- Common to both new C9350 & C9610
- Simplified cabling & dynamic link add/change
- Improved SSO and ISSU/SMU convergence

... and more, coming soon

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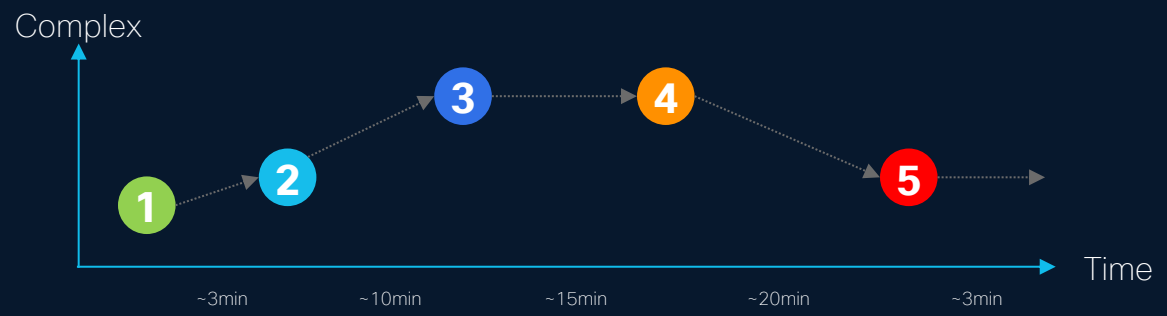
Agenda

1. Why do you need Stacking?
2. Brief history of Cisco Stacking
3. What is Cisco ‘Smart’ Stacking? NEW
4. Smart Stacking on C9350 & C9610 NEW
5. Designing with Smart Stacking NEW



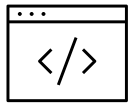
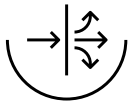
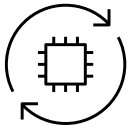
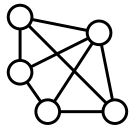
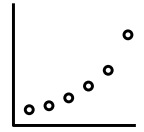
Cisco Smart Stacking

Why do you need Stacking?

Why do you need Stacking?

Key benefits for you & your network

TCO

Management & Operations	Resiliency & Convergence	Software Simplification	Topology Simplification	Bandwidth Utilization

Stacking

Simplified	Stateful (SSO/NSF)	Stateful Upgrades	Easy L2 & L3	Efficiency
Combines multiple physical switches in one logical entity: one device, one config file and one IP address.	Standby chassis has a "hot" copy of the control plane. Failover occurs in milliseconds - maintaining data sessions for minimal disruption.	Stateful in-service upgrades with ISSU or XFSU + NSF, for sub-second convergence. One upgrade for all switches.	Eliminates STP and HSRP/VRRP. Upstream and downstream devices see a single neighbor - reducing routing table complexity.	Uses Multi-Chassis EtherChannel (MEC) where all L2 or L3 links are forwarding simultaneously, doubling your bandwidth.

Traditional

Complexity	Protocol Dependent	Separate Upgrades	Difficult L2 & L3	Inefficient
Multiple separate switches to manage: multiple devices, multiple config files, and multiple IP addresses.	Uses HSRP/VRRP & ECMP for failover. Recovery depends on timers (often in seconds) and/or dropping sessions.	Switches are upgraded separately and rely on protocols to converge (based on timers). Requires multiple upgrades to complete.	Requires complex STP and First Hop redundancy configurations, plus multiple L2 & L3 adjacencies.	Relies on Spanning Tree Protocol (STP) to prevent L2 loops - which "blocks" redundant L2 links (50% of bandwidth is idle).

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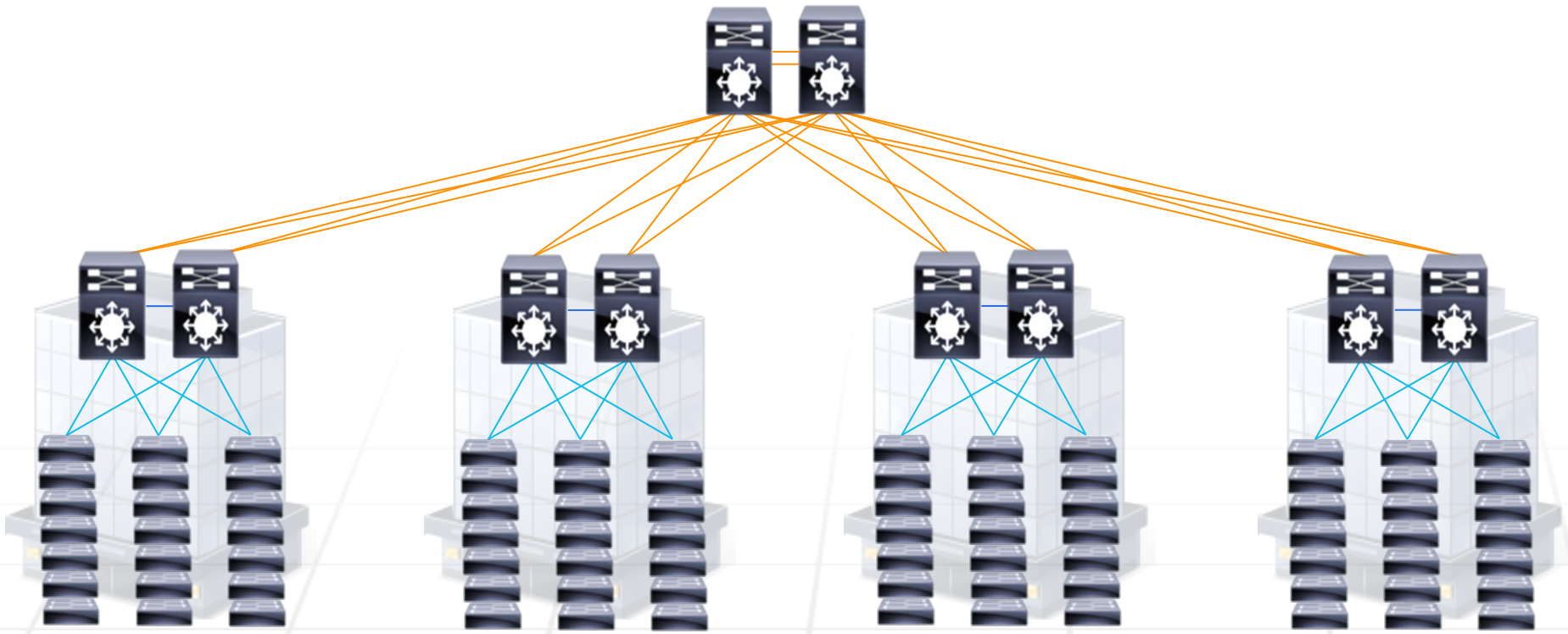
Traditional L2/L3 Network Design



Building 1
1000 Ports

Building 2
1000 Ports

Building 3
1000 Ports

Building 4
1000 Ports

Standalone Core

Standalone Access

Network Design
(4000 Access Ports)

94 Software & Licenses
94 Configurations
168 Port-Channels
168 Access Trunks

94 config variations:
Hostnames, VLANs, IP/masks, SNMP, RADIUS, NETCONF, etc.

Extra Considerations:

- STP Loop Prevention
- CAM & ARP Tuning
- FHRP Tuning / Priority
- Routing Protocol Tuning
- PIM Tuning / DR priority

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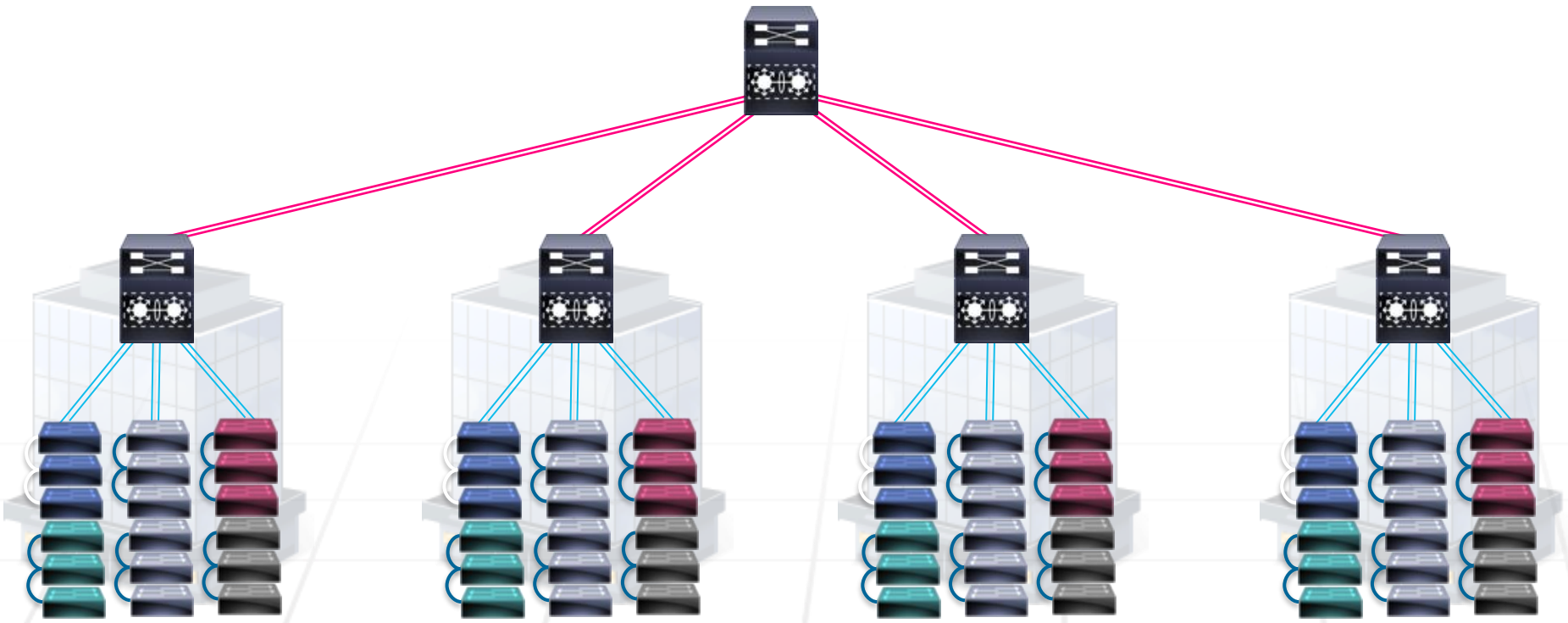
Stackwise + Stackwise Virtual



Building 1
1000 Ports

Building 2
1000 Ports

Building 3
1000 Ports

Building 4
1000 Ports

Stacked Core

Stacked Access

Network Design
(4000 Access Ports)

25 Software & Licenses
25 Configurations
24 Port-Channels
24 Access Trunks

25 config variations:
Hostnames, VLANs, IP/masks, SNMP, RADIUS, NETCONF, etc.

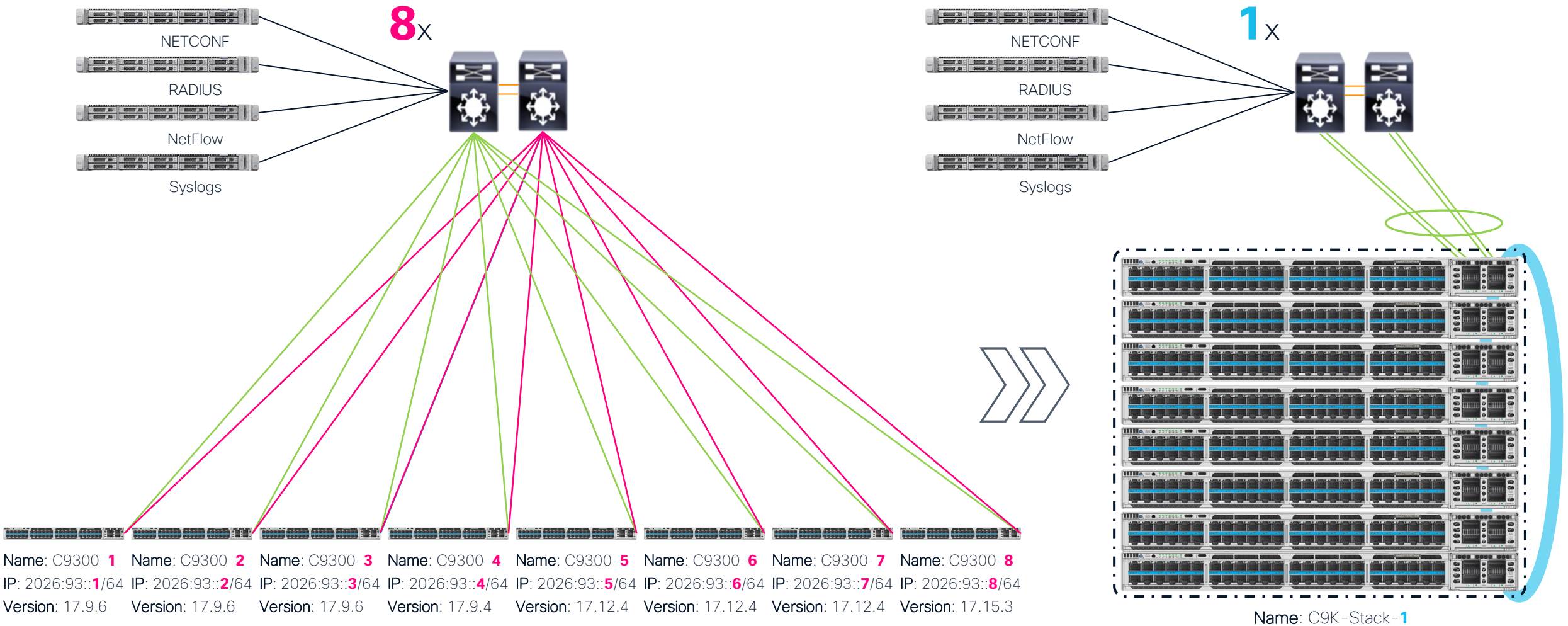
Extra Considerations:

- ~~STP Loop Prevention~~
- ~~CAM & ARP Tuning~~
- ~~FHRP Tuning / Priority~~
- ~~Routing Protocol Tuning~~
- ~~PIM Tuning / DR priority~~

Stacking simplifies your Management

1000 switches / 8 = 125 switches

Single Management Point – Less IPs, Configs, Upgrades, Syslogs, NetFlow, RADIUS, SNMP & NETCONF, etc., etc.



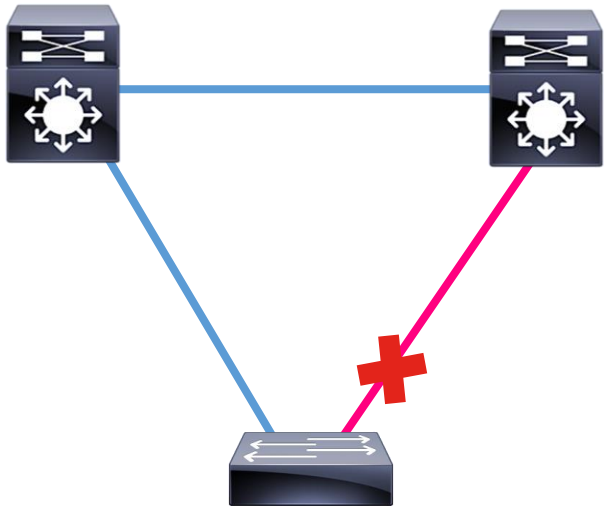
Stacking simplifies your Topology

The power of Multi-chassis EtherChannel (MEC)

A primary goal is to use **Multi-chassis EtherChannel (MEC)**

a single Portchannel to multiple physical switches

From this:



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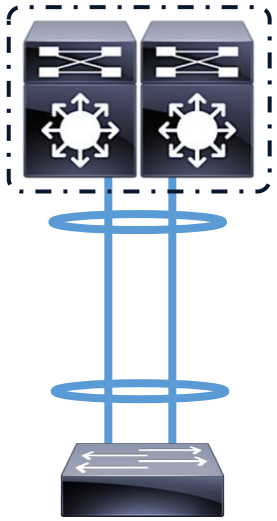
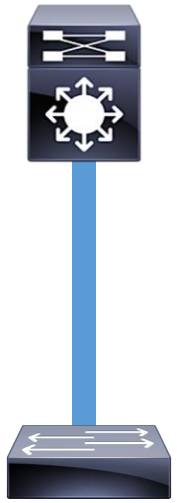


or logically:



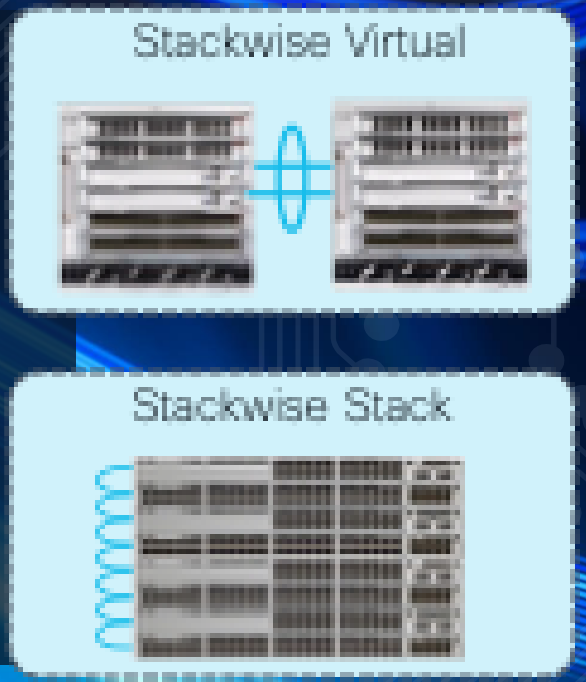
Stacking simplifies your Configurations

Single Config with Fewer Protocols

Standalone Core 1	Standalone Core 2	SVL Core (single config)
L2 Spanning Tree Configuration		
! Enable 802.1d per VLAN spanning tree enhancements. **spanning-tree mode rapid-pvst** spanning-tree extend system-id **spanning-tree loopguard default** **spanning-tree uplinkfast** **spanning-tree backbonefast** ! Enable STP root for VLAN load-splitting. **spanning-tree vlan 2,4,6,8,10,200-400 priority 24576** **spanning-tree vlan 1,3,5,7,9,100-300 priority 32768**	! Enable 802.1d per VLAN spanning tree enhancements. **spanning-tree mode rapid-pvst** spanning-tree extend system-id **spanning-tree loopguard default** **spanning-tree uplinkfast** **spanning-tree backbonefast** ! Enable STP root for VLAN load-splitting. **spanning-tree vlan 2,4,6,8,10,200-400 priority 32768** **spanning-tree vlan 1,3,5,7,9,100-300 priority 24576**	! Enable 802.1d per VLAN spanning tree enhancements **spanning-tree mode rapid-pvst** spanning-tree extend system-id
L3 VLAN IP Configuration		
! Define the Layer 3 SVI for each voice and data VLAN **interface Vlan4** **ip address 10.120.4.2 255.255.255.0** no ip redirects no ip unreachables load-interval 30 ! Enable PIM and Reduce query interval to 250 msec **ip pim sparse-mode** **ip pim query-interval 250 msec** ! Define HSRP default gateway with 250/800 msec hello/hold **standby 1 ip 10.120.4.1** **standby 1 timers msec 250 msec 800** ! Set preempt delay large enough to allow network to stabilize ! before HSRP switches back on power on or link recovery **standby 1 preempt delay minimum 180** ! Enable HSRP authentication **standby 1 authentication cisco123**	! Define the Layer 3 SVI for each voice and data VLAN **interface Vlan4** **ip address 10.120.4.3 255.255.255.0** no ip redirects no ip unreachables load-interval 30 ! Enable PIM and Reduce query interval to 250 msec **ip pim sparse-mode** **ip pim query-interval 250 msec** ! Define HSRP default gateway with 250/800 msec hello/hold **standby 1 ip 10.120.4.1** **standby 1 timers msec 250 msec 800** ! Set preempt delay large enough to allow network to stabilize ! before HSRP switches back on power on or link recovery **standby 1 preempt delay minimum 180** ! Enable HSRP authentication **standby 1 authentication cisco123**	! Define the Layer 3 SVI for each voice and data VLAN **interface Vlan4** **ip address 10.120.4.1 255.255.255.0** no ip redirects no ip unreachables **ip pim sparse-mode** load-interval 30

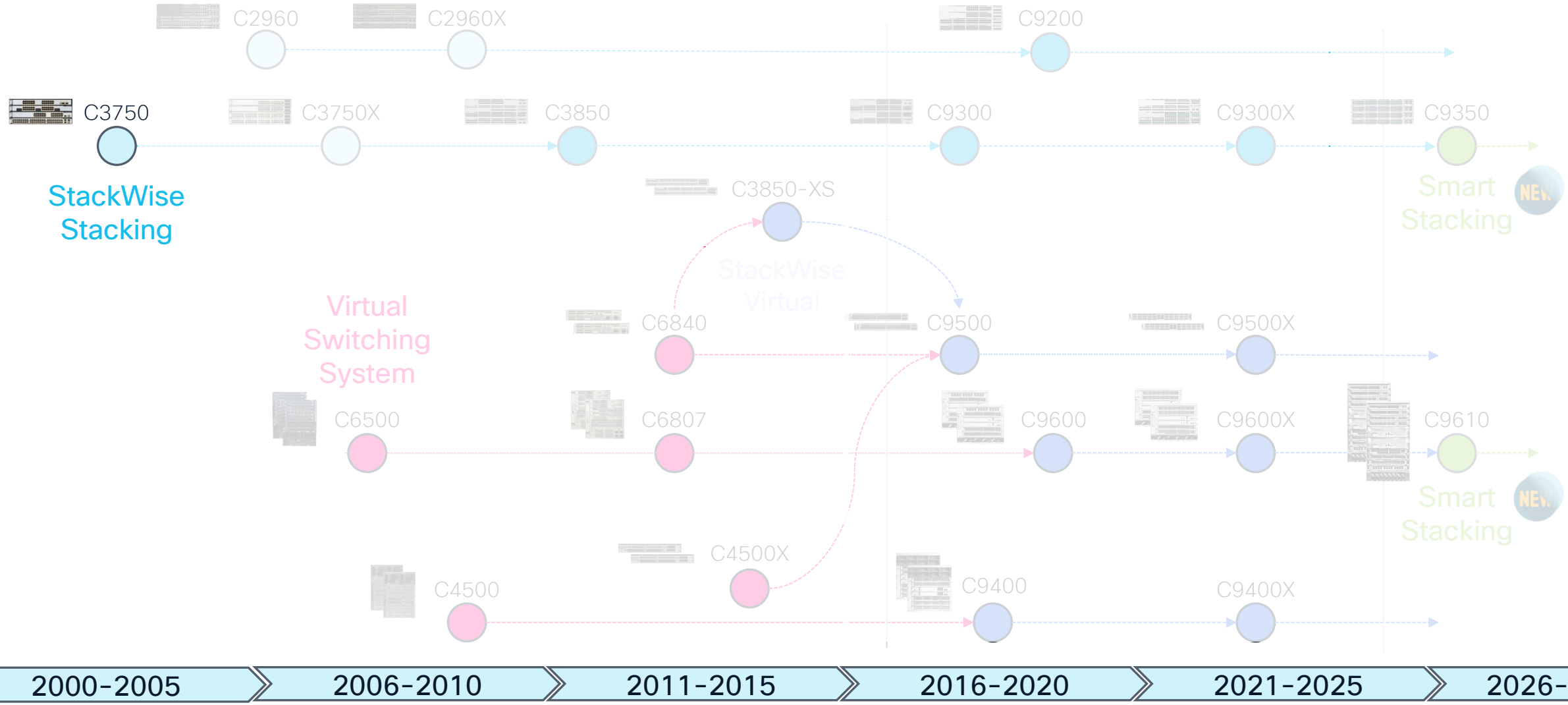
Cisco Smart Stacking

Brief History of Cisco Stacking



A brief history of Cisco Stacking

Basic Timeline & Milestones



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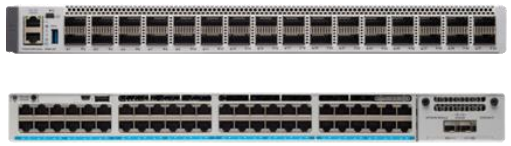
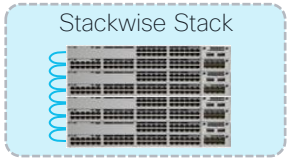
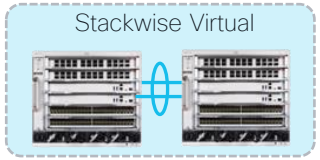
C9K Fixed vs. Modular vs. Stacking

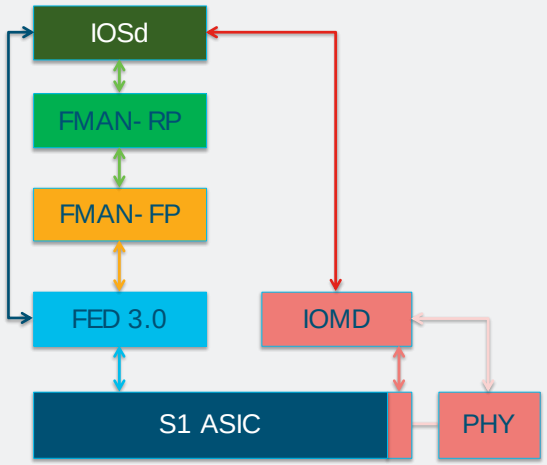
Reusing common OS infrastructure components



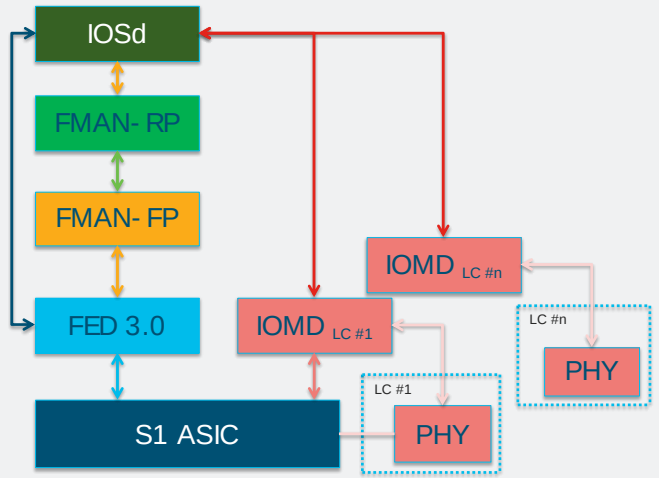




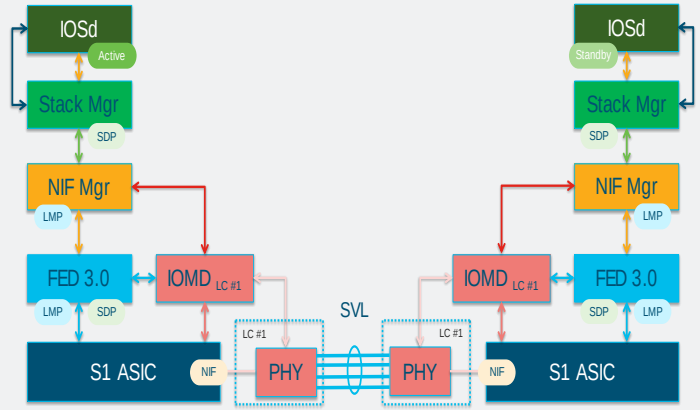
Fixed Platform



Modular Platform



Stacked Platform(s)

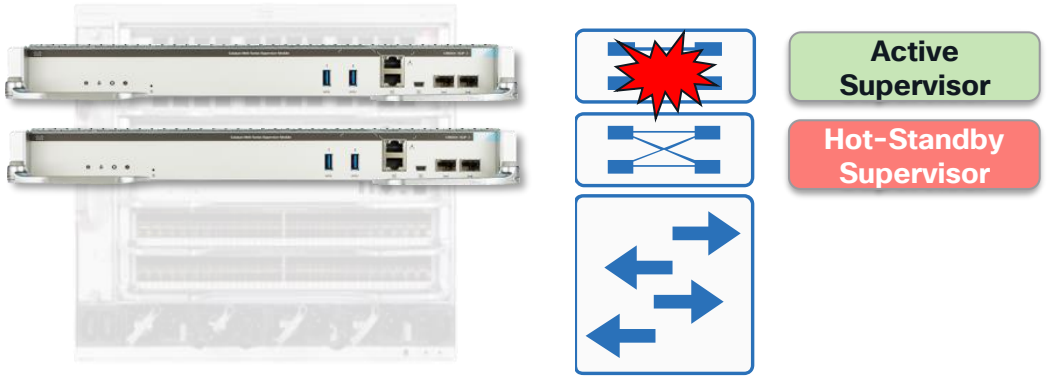


Understanding High-Availability

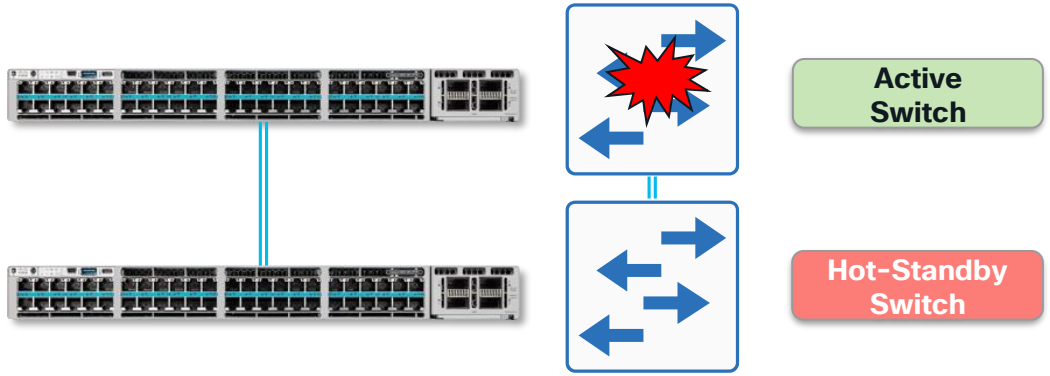
Stateful Switchover (SSO) and Non-Stop Forwarding (NSF)

- **Stateful Switchover** (SSO) synchronizes active process state and running-config, between Active & Standby supervisors or Active & Standby switches in a stack
  - Traffic loss minimized for Active supervisor or Active switch failure
- **Non-Stop Forwarding** (NSF) allows for graceful restart of L3 routing protocols

Modular Switch with **Redundant Supervisors**



StackWise Stack or **StackWise Virtual Pair**



Cisco Stackwise

Access Switch Stacking

Catalyst 9300 Series

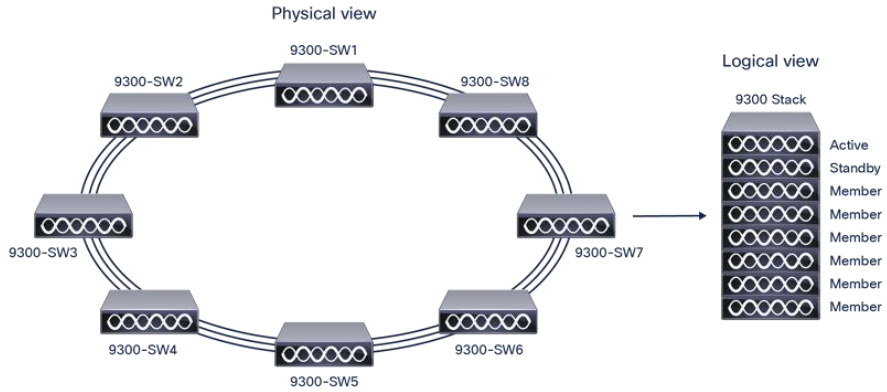
Catalyst 9200 Series

Cisco StackWise technology

Manage one logical switch - with up to 8 physical switches

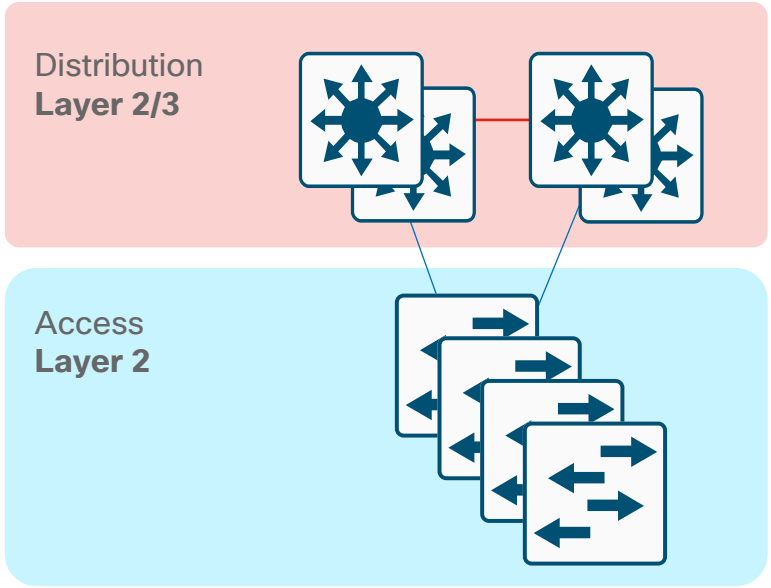
Catalyst 9200/L Series StackWise-160/80

- Catalyst 9200 Series stacking of up to 8 switches and 416 ports
  - StackWise-160 is supported on Catalyst 9200 switch models
  - StackWise-80 is supported on Catalyst 9200L switch models



Catalyst 9300/L Series StackWise-480/360

- Catalyst 9300 Series stacking of up to 8 switches and 448 ports
  - StackWise-480 is supported on Catalyst 9300 switch models
  - StackWise-360 is supported on Catalyst 9300L switch models



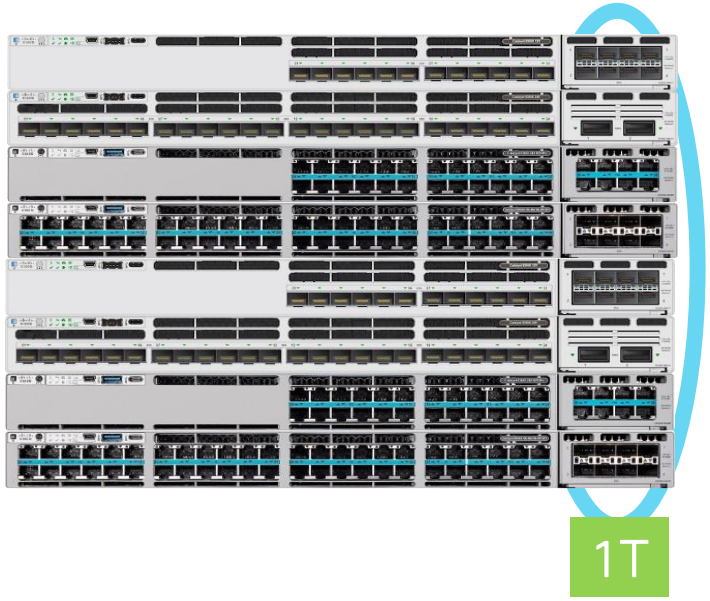
Catalyst 9300X/LM Series StackWise-1T

- Catalyst 9300X Series stacking of up to 8 switches and 448 ports

Catalyst 9300 Series – StackWise 1T, 480 & 320

Common ring-based Stacking architecture

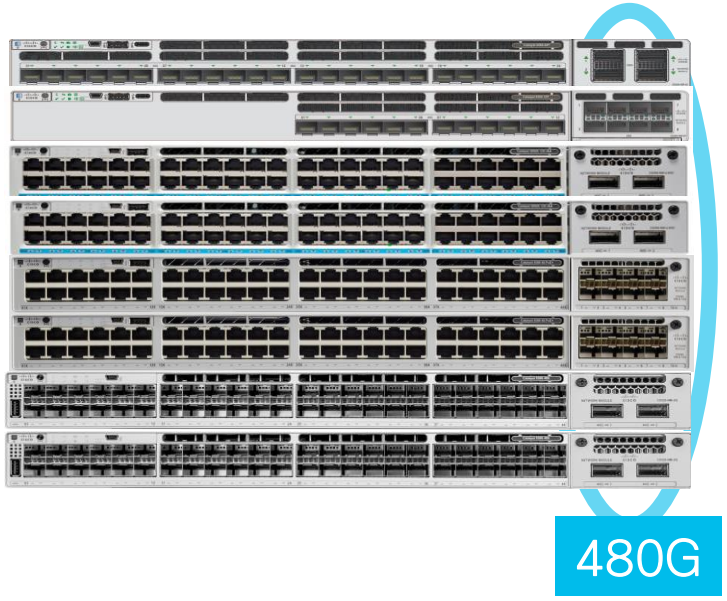
Modular Uplink
C9300X SKUs



8 switches

1T

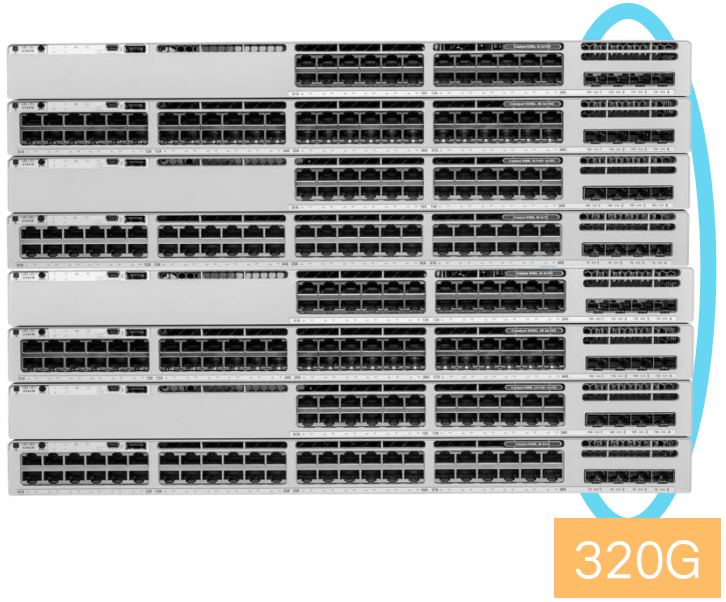
Modular Uplink
C9300 SKUs



8 switches

480G

Fixed Uplink
C9300L SKUs



8 switches

320G

Stacking supported among C9300X SKUs (1T)

Stacking supported among C9300 SKUs (480G)

and 'Mixed Stacking' between C9300 and C9300X SKUs (480G)

Stacking supported among C9300L SKUs only

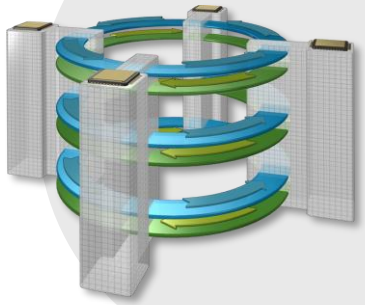
STACK-T1

STACK-T3

Catalyst 9300 Series – StackWise 1T, 480 & 320

Understanding Stack Bandwidth

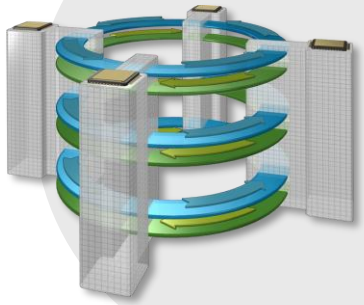
C9300X SKUs
Modular Uplinks



- **6 rings** in Total
  - 3 rings go East
  - 3 rings go West
- Each ring is **90 Gbps**
- 540G Unidirectional
- **1080G** Spatial Reuse

6 x 90G = 540G x 2 = 1080G

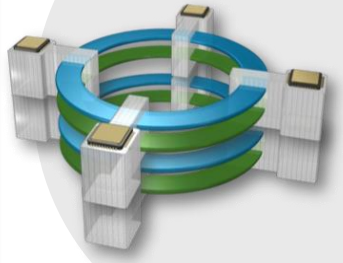
C9300 SKUs
Modular Uplinks



- **6 rings** in Total
  - 3 rings go East
  - 3 rings go West
- Each ring is **40 Gbps**
- 240G Unidirectional
- **480G** Spatial Reuse

6 x 40G = 240G x 2 = 480G

C9300L SKUs
Fixed Uplinks



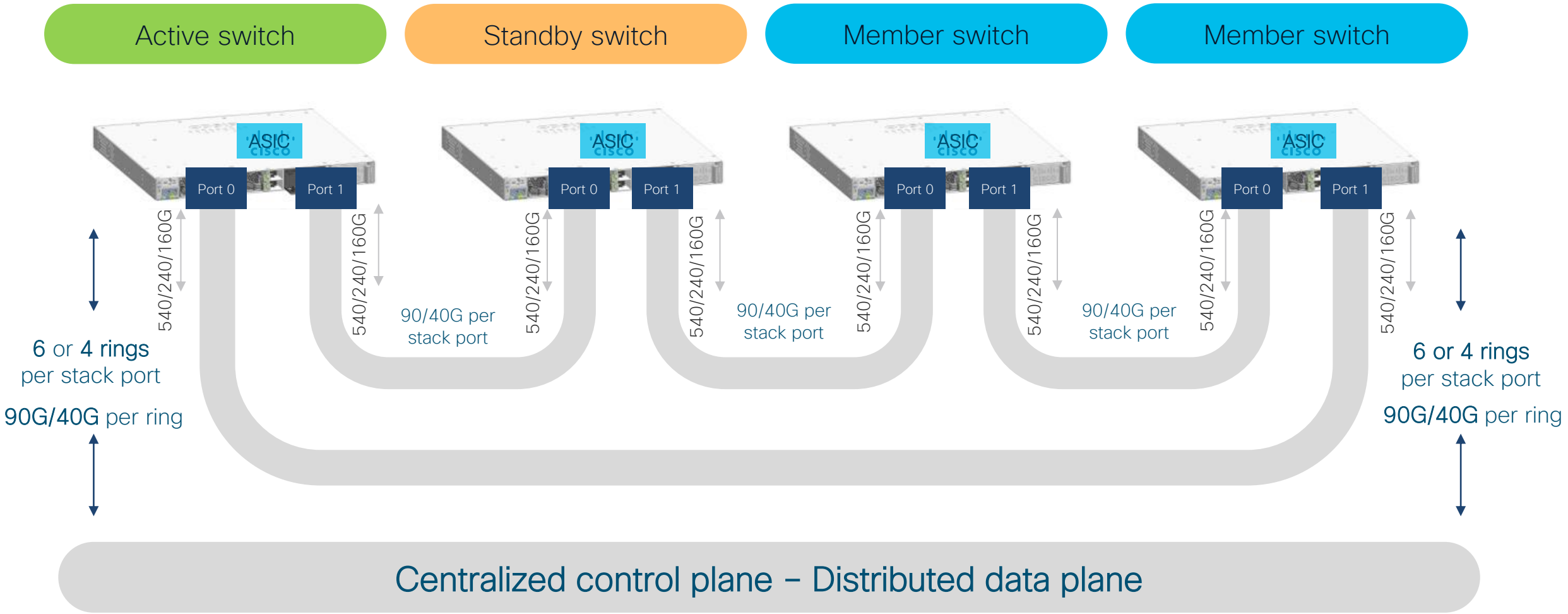
- **4 rings** in Total
  - 2 rings go East
  - 2 rings go West
- Each ring is **40 Gbps**
- 160G Unidirectional
- **320G** Spatial Reuse

4 x 40G = 160G x 2 = 320G

Spatial Reuse = transmit unicast traffic in **both directions** (1x East + 1x West)

Catalyst 9300 Series – StackWise 1T, 480 & 320

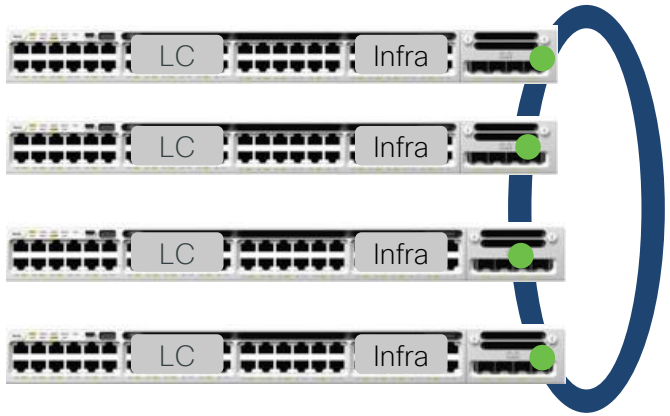
Understanding Stack Bandwidth

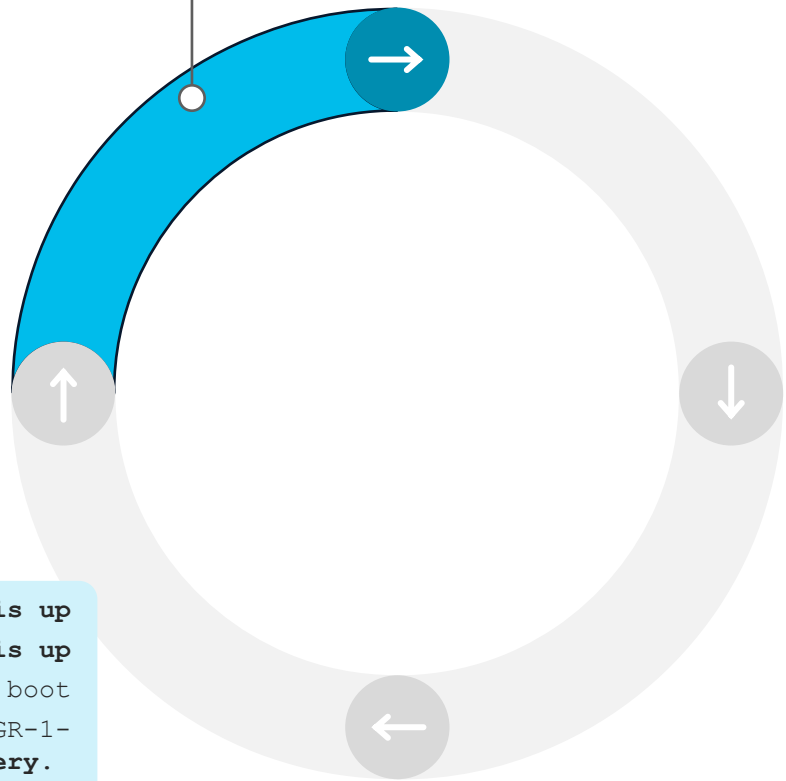


Stacking Process – Stack discovery

Stack discovery

- Broadcast, followed by neighborcast





Stack Interfaces brought online

Stack Discovery Protocol runs

Full Ring: Discovery exits after all members are found

Half Ring: System waits for 2 min

```
Stack port 1 cable is connected and the link is up
Stack port 2 cable is connected and the link is up
Waiting for 120 seconds for other switches to boot
%IOSXE-1-PLATFORM: process stack-mgr: %STACKMGR-1-DISC_START: Switch 3 is starting stack discovery.
##All switches in the stack have been discovered
```

```
Switch number is 3
%IOSXE-1-PLATFORM: process stack-mgr: %STACKMGR-1-DISC_DONE: Switch 3 has finished stack discovery.
%IOSXE-1-PLATFORM: process stack-mgr: %STACKMGR-1-SWITCH_ADDED: Switch 3 has been added to the stack.
```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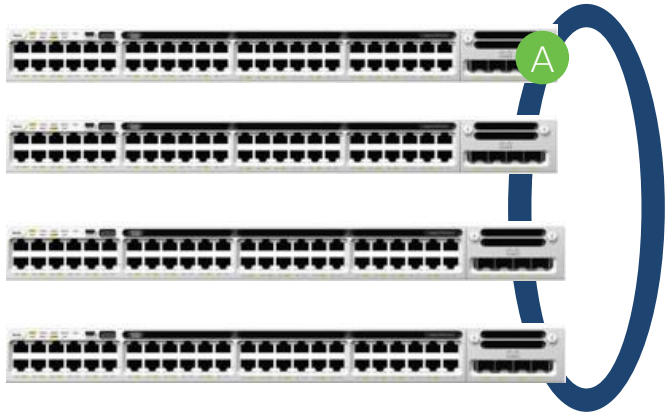
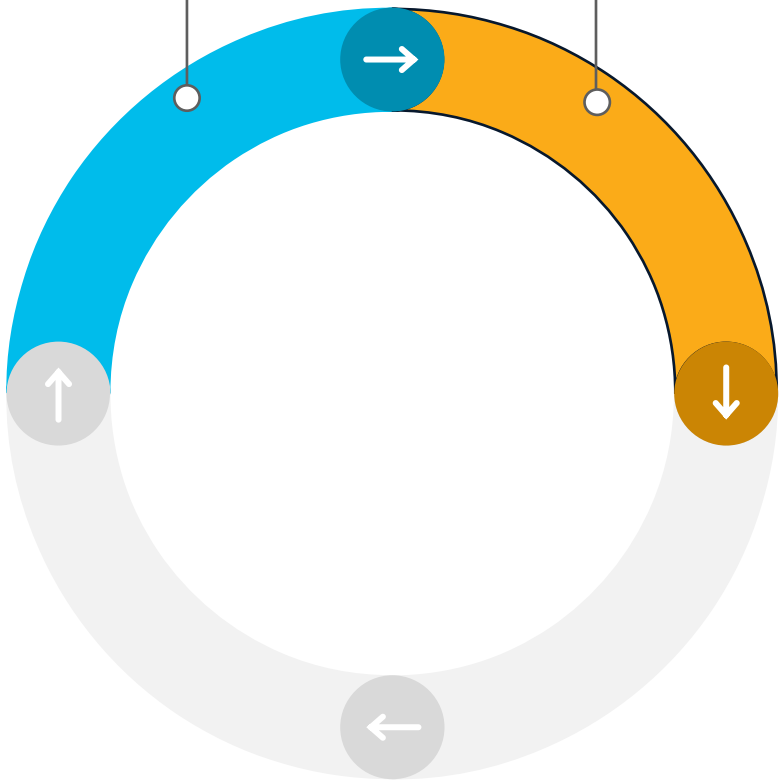
Stacking Process – Stack Active election

Stack discovery

- Broadcast, followed by neighborcast





Stack active election

- Lowest MAC address

Stack member that has the **lowest** MAC address

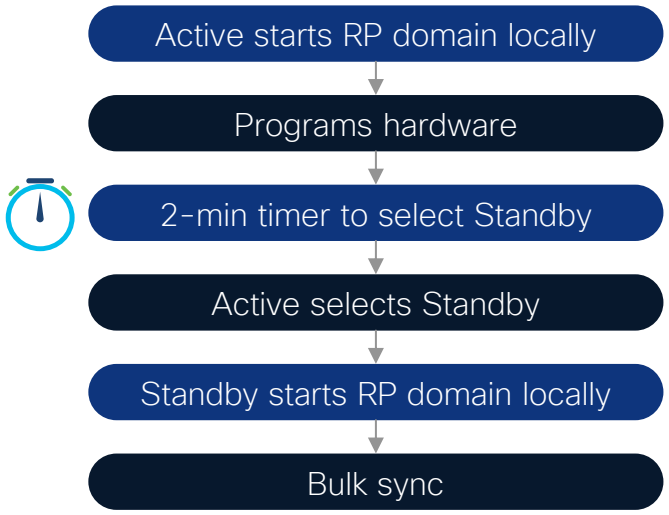
Switch with **highest** user-configured **priority** (1–15)

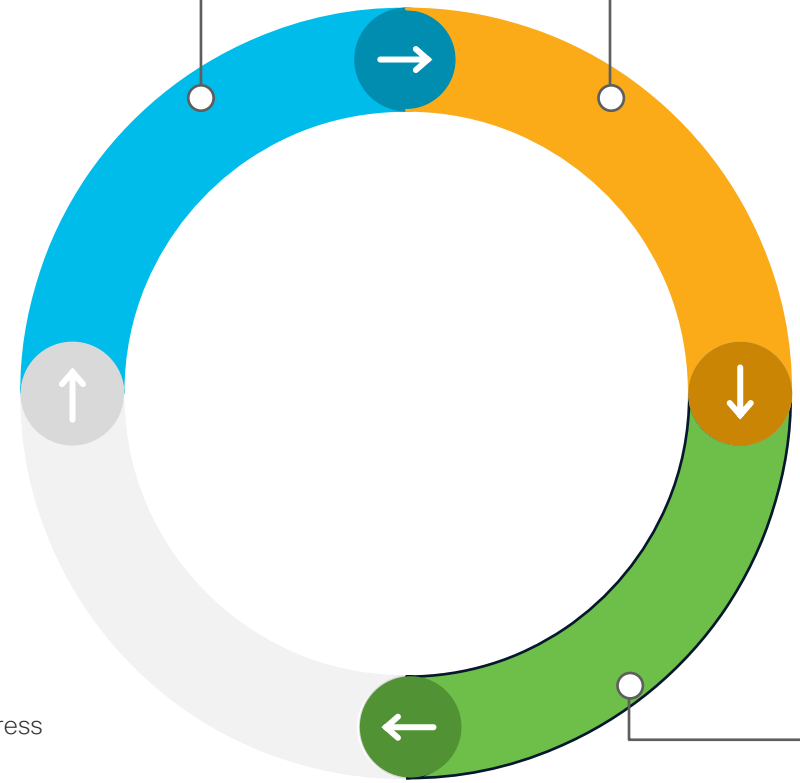
```
%IOSXE-1-PLATFORM: process stack-mgr: %STACKMGR-1-ACTIVE_ELECTED: Switch 3 has been elected ACTIVE.
```

Stacking Process – Stack initialization

Stack discovery

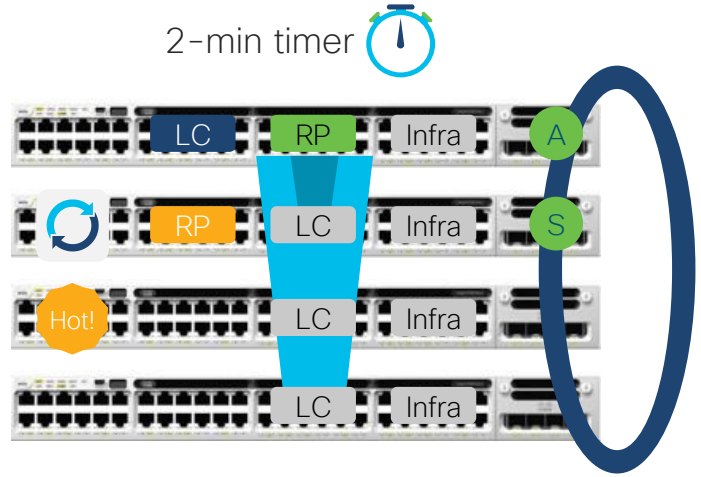
- Broadcast, followed by neighborcast





Stack active election

- Lowest MAC address



Stack initialization

- Active starts RP domain

Switch# show switch
Switch/stack MAC address: 2037.0652.a580 - local MAC address
MAC persistency wait time: Indefinite
H/W current

Switch#	Role	MAC address	Priority	Version	State
1	Member	2037.0653.ca80	5	P6A	Ready
2	Standby	2037.0653.db00	10	P6A	Ready
3*	Active	2037.0652.a580	15	V01	Ready

Stacking Process – Stack member addition

Stack discovery

- Broadcast, followed by neighborcast

Stack discovery initiated

↓

Complete full ring

↓

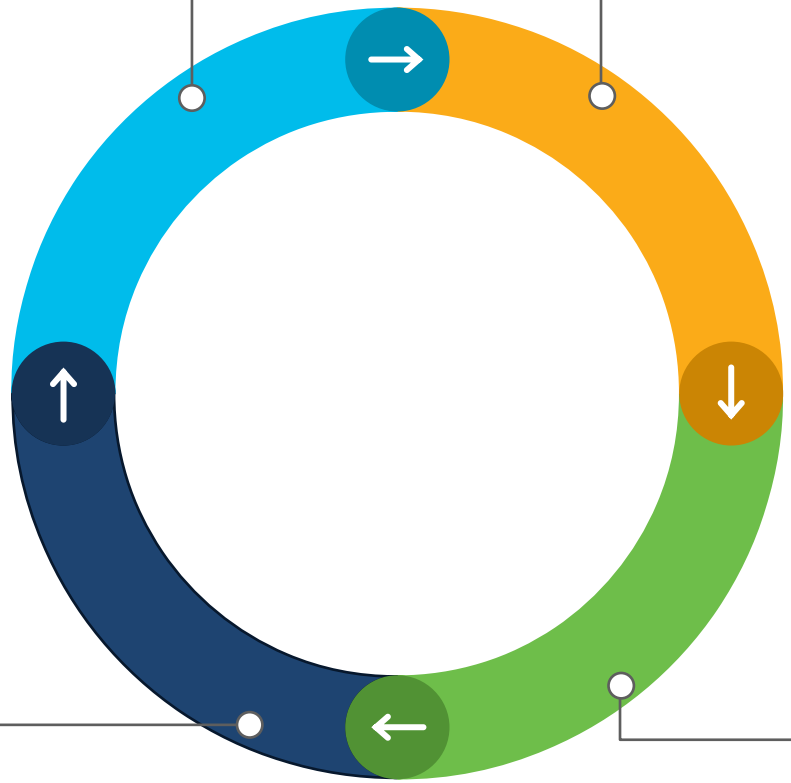
Active detects new addition

↓

Active is not preempted by high-priority member

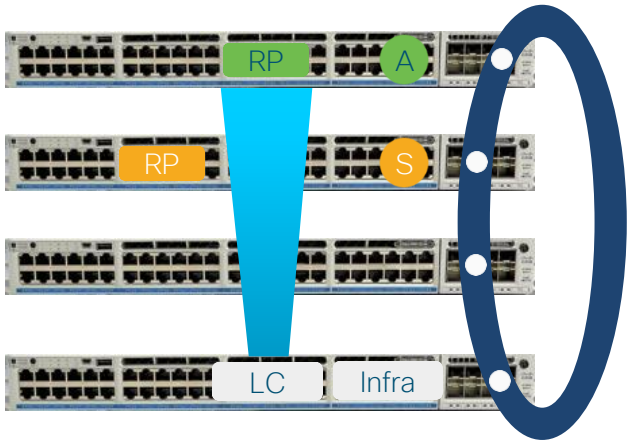
Stack member addition

- Stack discovery initiated



Stack active election

- Lowest MAC address



Stack initialization

- Active starts RP domain

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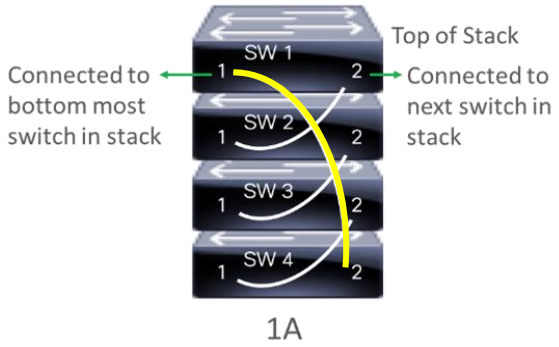
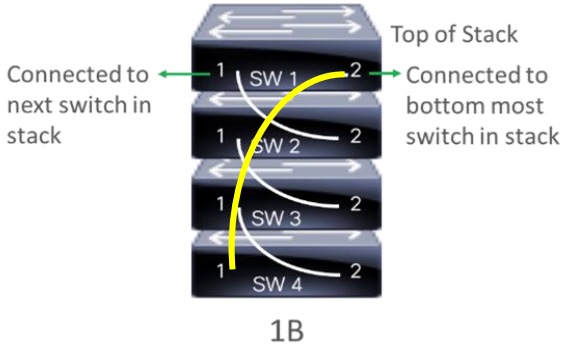
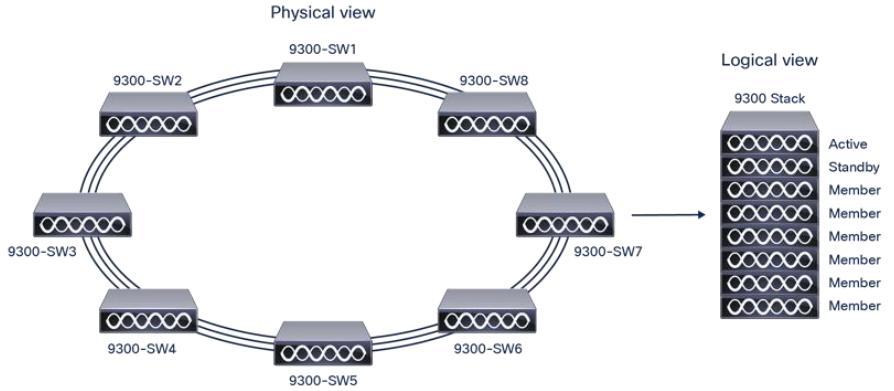
Stacking Process – Stack Cabling

Stackwise is a Ring topology: Only 2 Cable Configurations

Supported Stack Ring designs





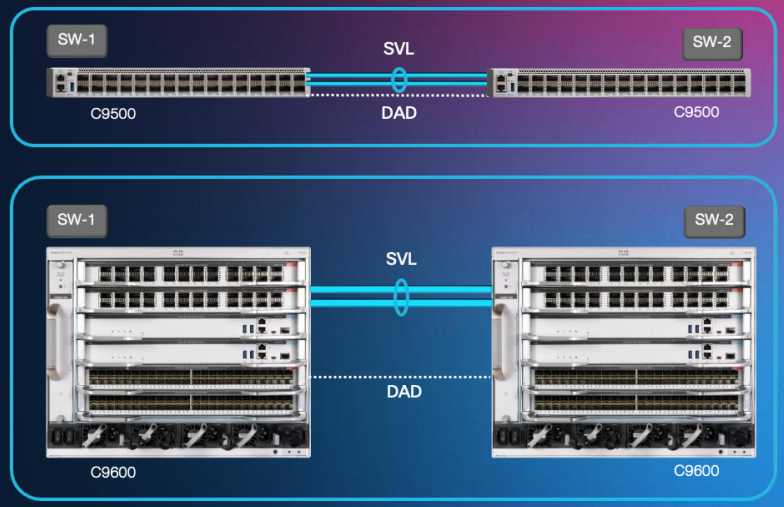


community.cisco.com/t5/switching/9300-stackwise-cableing-order/td-p/4480659

1. **Start without stacking cables.** if a stack cable is detected during boot, the stack master will wait for the rest of stack members to boot up. This prolongs the process by (a minimum) of two minutes.
2. **Power up Switch 1.**
3. **Look at the front panel:** wait for the two left-most LEDs, one on top of another, to start blinking. When this happens - connect ONE stacking cable to switch 2 and power up switch 2.
4. **Repeat with Switch 2.**
   Rinse. Repeat. Et cetera
5. **Once all Switch members are up:** then connect the "return" stacking cable (last switch to first).

Cisco Stackwise Virtual

Core/Distribution Switch Stacking



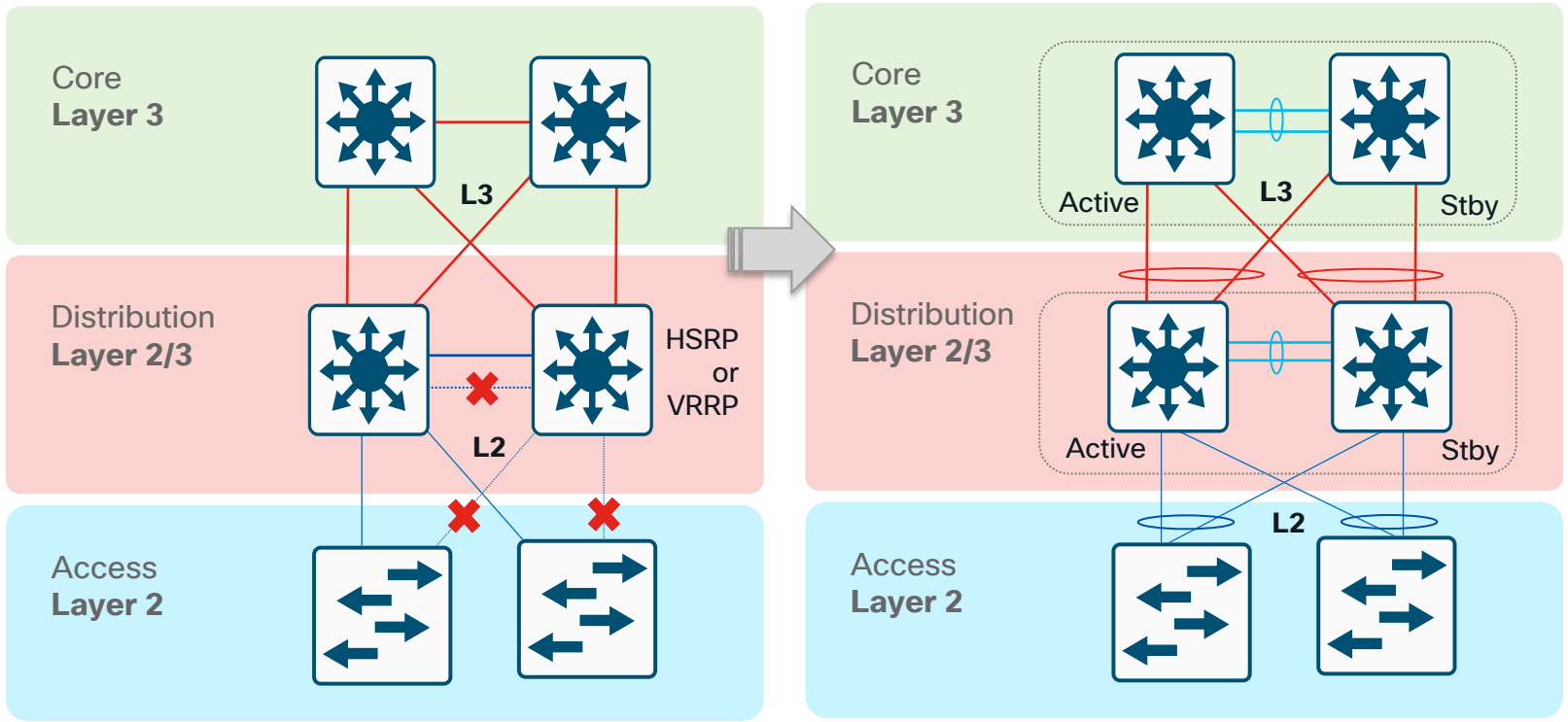
StackWise Virtual Technology

- Intended for **Distribution** and **Core** layer
- Available on **C9400**, **C9500** and **C9600**
- Formed using **Front Panel** ethernet ports

Catalyst 9600/X Catalyst 9500/X Catalyst 9400/X

up to 8x
10/25/50G SFP

up to 8x
40/100/400G QSFP



- **Simplify Operations** by Eliminating STP, FHRP and Multiple Touch-Points
- **Double Bandwidth** and Reduce Latency with Active-Active Multi-chassis EtherChannel (MEC)
- **Minimize Convergence** with Sub-second Stateful and Graceful Restart (SSO/NSF)

StackWise Virtual

Distribution & Core Switch Stacking

Catalyst 9600/X

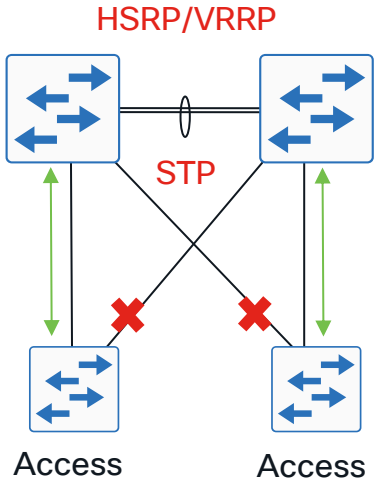
Catalyst 9500/X

Catalyst 9400/X

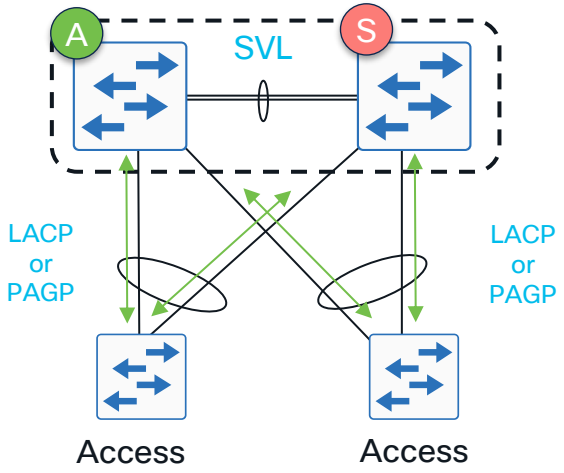
SSO Active is responsible for:

- Management
- L2 protocols
- L3 protocols

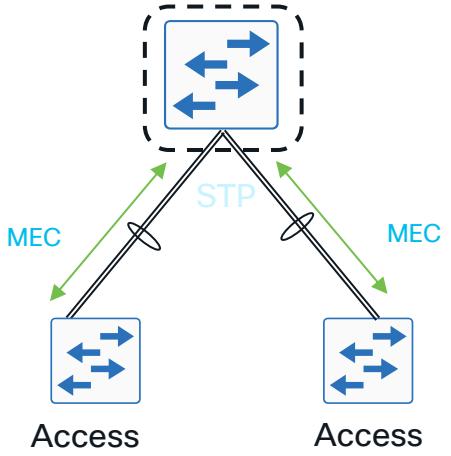
Traditional L2/L3



StackWise Virtual - **Physical**



StackWise Virtual - **Logical**



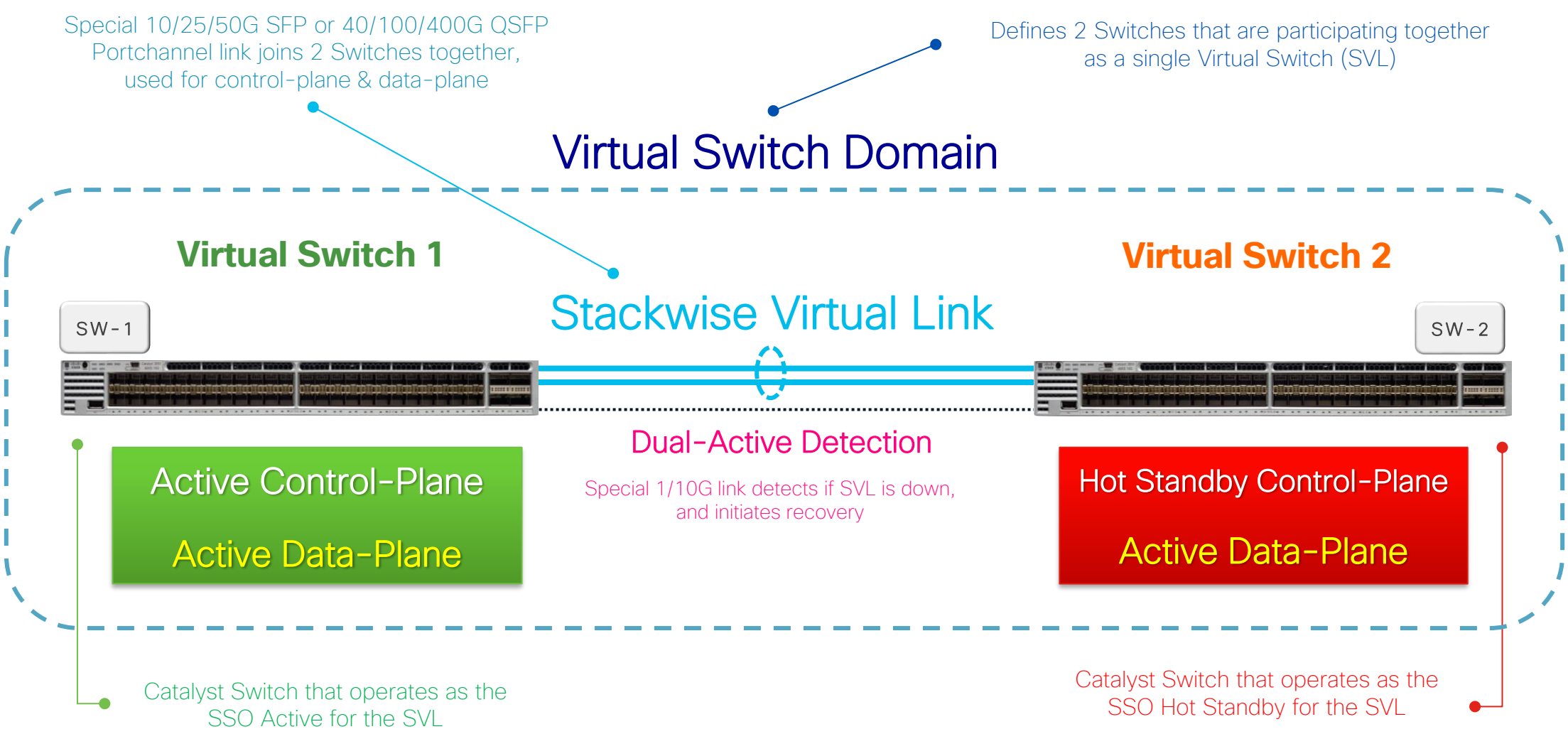
Both Active & Standby switches have Active/Active data-plane and make forwarding decisions

StackWise Virtual

Key Concepts of SVL

Special 10/25/50G SFP or 40/100/400G QSFP Portchannel link joins 2 Switches together, used for control-plane & data-plane

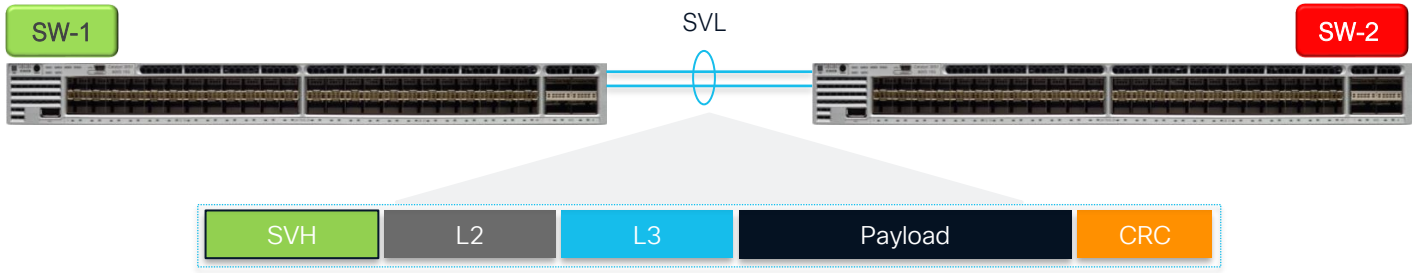
Defines 2 Switches that are participating together as a single Virtual Switch (SVL)



StackWise Virtual Link (SVL)

SVL Interface characteristics

- **Inter-Chassis System Link**
  - No additional network protocols
  - Invisible in the network topology
  - Transparent to network level troubleshooting
- **SVL Control Link**
  - Carries all internal system control traffic
  - dynamic election during bootup
  - Shared interface for network/data traffic
- **Payload Overhead**
  - Every packet encapsulated with 64B of StackWise Virtual Header (SVH)
  - SVL must be directly connected between two stack-member switch systems




```
C9K-Dist-1# show stackwise-virtual link

Stackwise Virtual Link(SVL) Information:
-----------------------------------------------
Flags:
--------
Link Status
--------------
U-Up D-Down
Protocol Status
-------------------
S-Suspended P-Pending E-Error T-Timeout R-Ready
-----------------------------------------------------------------
Switch    SVL     Ports                     Link-Status    Protocol-Status
------    ---     -----                     -----------    ---------------
1         1       HundredGigabitEthernet1/1/1   U          R
                  HundredGigabitEthernet1/1/2   U          R
2         1       HundredGigabitEthernet2/1/1   U          R
                  HundredGigabitEthernet2/1/2   U          R
```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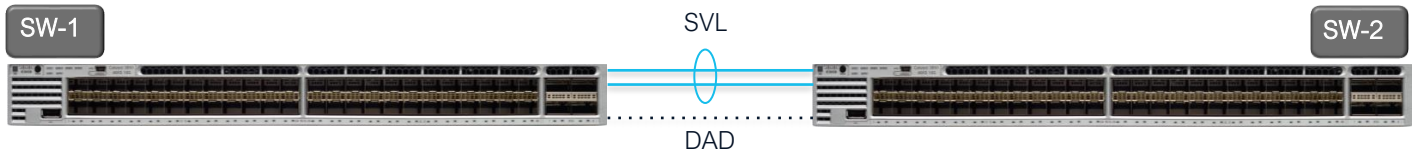
StackWise Virtual

Putting it all together



SW-1	SW-2
C9K-Dist-1(config)# **stackwise-virtual**	C9K-Dist-2(config)# **stackwise-virtual**
C9K-Dist-1(config)# **domain** <1-255>	C9K-Dist-2(config)# **domain** <1-255>

SW-1	SW-2
C9K-Dist-1(config)# **interface range** Hun x/y/z	C9K-Dist-2(config)# **interface range** Hun x/y/z
C9K-Dist-1(config-if)# **stackwise-virtual link** <1 | 255>	C9K-Dist-2(config-if)# **stackwise-virtual link** <1 | 255>

SW-1	SW-2
C9K-Dist-1(config)# **interface range** Gig x/y/z	C9K-Dist-2(config)# interface range Gig x/y/z
C9K-Dist-1(config-if)# **stackwise-virtual dual-active-detection**	C9K-Dist-2(config-if)# **stackwise-virtual dual-active-detection**

SW-1	SW-2
C9K-Dist-1# copy run start	C9K-Dist-2# copy run start
C9K-Dist-1# reload	C9K-Dist-2# reload

Step 1: StackWise Virtual Domain

- Enable StackWise Virtual
- Configure StackWise Domain–ID (Default=1. Optional Range 1-255)

Step 2: StackWise Virtual Link

- Configure StackWise Virtual Links
- Assign physical ports to SVL interface (Default=128. Optional Range 1-255)
- Max 8 SVL member-links

Step 3: Dual-Active Detection

- Assign physical ports to DAD interface
- Max 4 Dual Active Fast Hello links

Step 4: Save and Reload

- Copy running configuration to startup
- Reload both system to enable (system will boot in SVL mode)

Designing HA with Cisco C9K

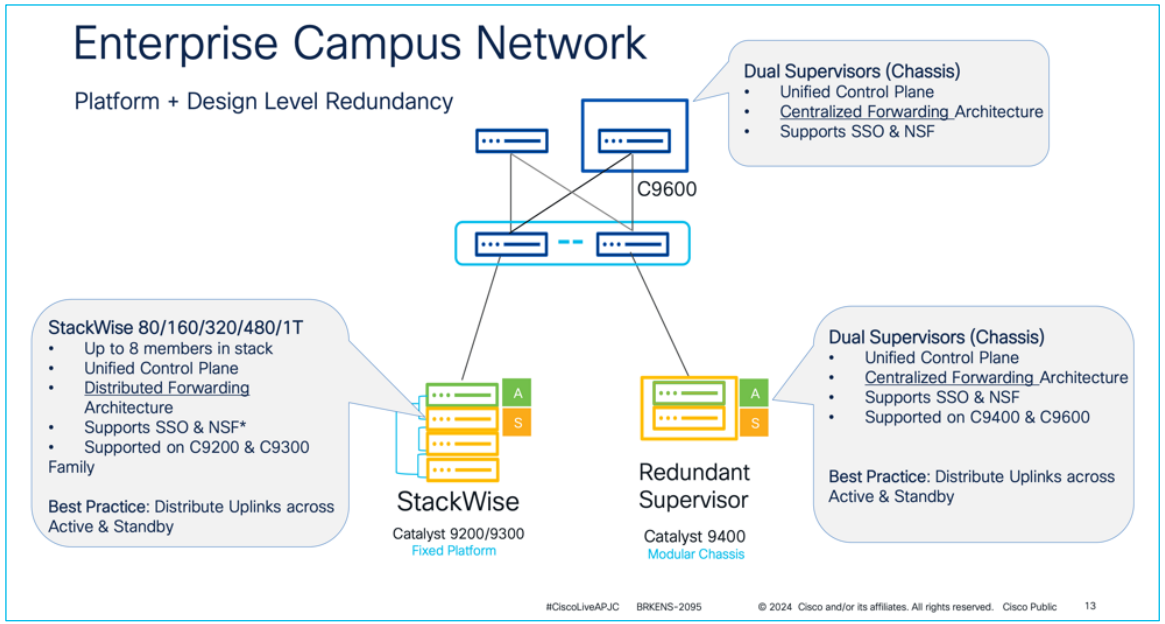
BRKENS-2095

Designing Highly Available Networks using Catalyst 9000 Series Switches

This session will cover new and existing high availability features introduced in IOS-XE on Catalyst 9000 Series switching platforms. We will discuss how you can achieve high availability in your network through various stages in the design lifecycle.

During the initial design, we will discuss the benefits of features like StackPower, power resiliency modes, StackWise-480 and StackWise Virtual. After the design phase, we will discuss features like GIR, extended fast software upgrade (xFSU), patchability, and ISSU that will help maintain resiliency during the operational phase.

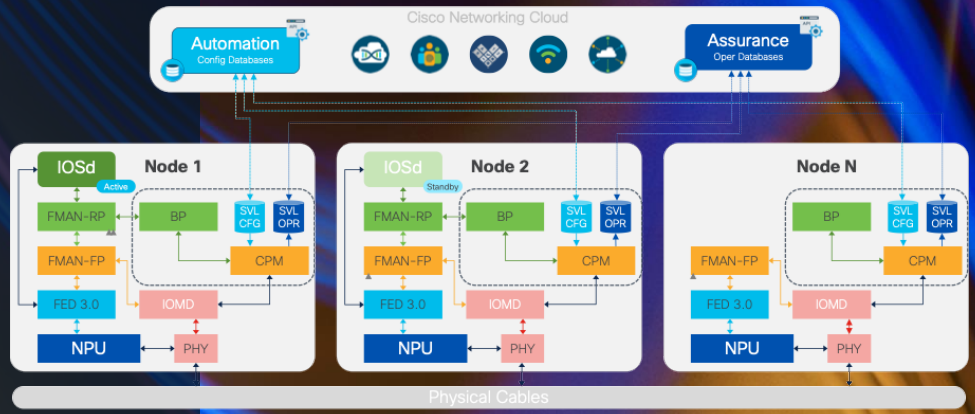
We will then conclude by covering how you can efficiently leverage all the high-availability features in different network designs and achieve maximum uptime and resiliency.



Cisco Smart Stacking

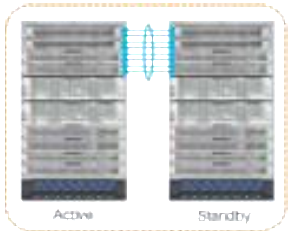
What is Smart Stacking?

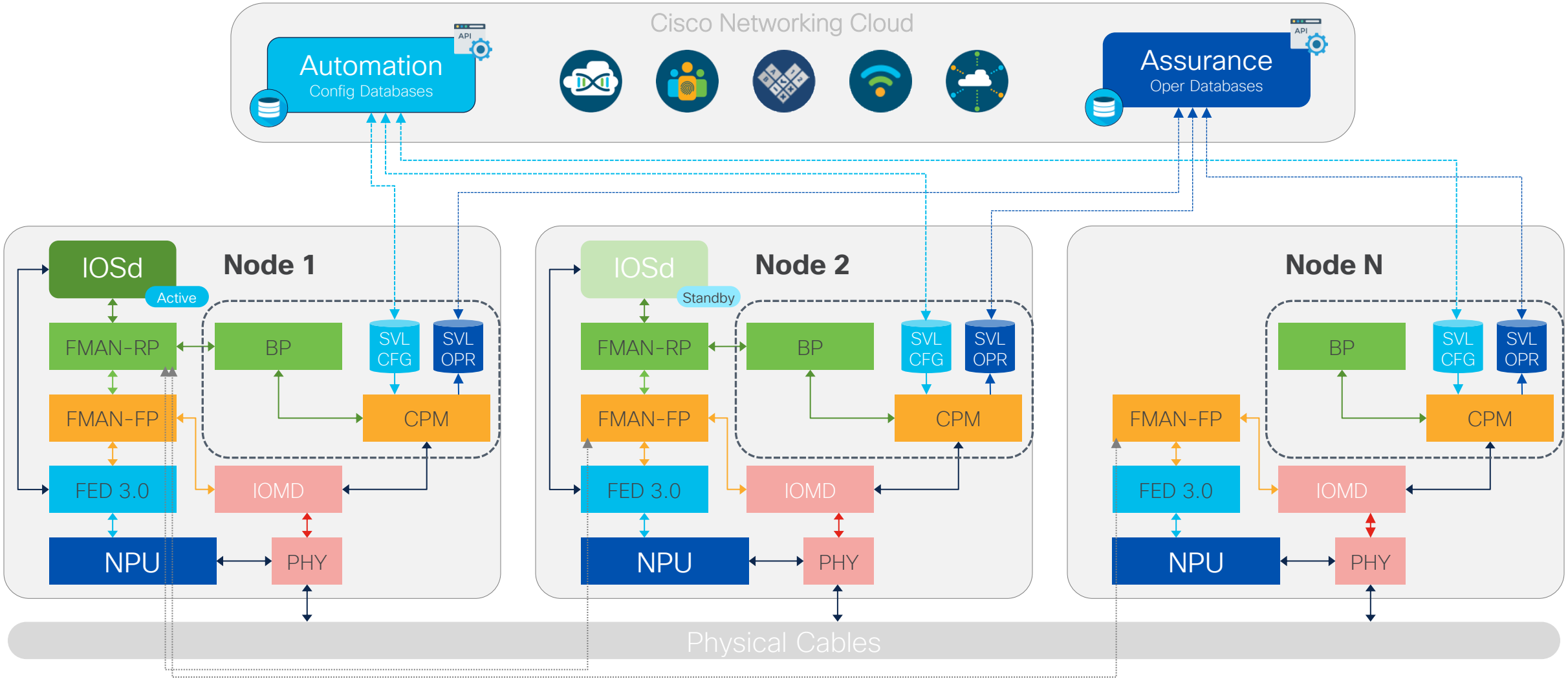
on Cisco C9K Smart Switches



What is Smart Stacking (NG-SVL)

An entirely new Stacking Architecture for Cisco C9K Smart Switches





NOTE: Simplified Diagram

1

What's inside of a

Cisco C9K Smart Switch

INTRODUCING

Cisco C9000 Series Smart Switches

Powerful, secure, easy to manage

Cisco Silicon One – industry's most powerful, programmable ASICs

High-performance, Multi-core x86 CPU & DRAM

Cisco IOS XE w/ Next-Generation Stacking & SVL

Secure On-device App Hosting

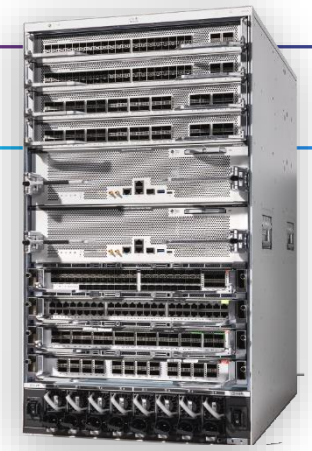
Universal PoE+ Perpetual PoE & PoE Analytics

Post-Quantum Secure Boot & Trustworthy Solution

Cisco C9350 Smart Switch

1.6 Tbps	4x100G	PQC	4x
Stacking bandwidth	*Uplink Modules*	*Post-Quantum Security*	*Higher MAC & ARP scale*

Cisco C9610 Smart Switch



25.6 Tbps	256x100G	PQC	10 slot
System bandwidth	*Modular Line-Cards*	*Post-Quantum Security*	*To power Core density*

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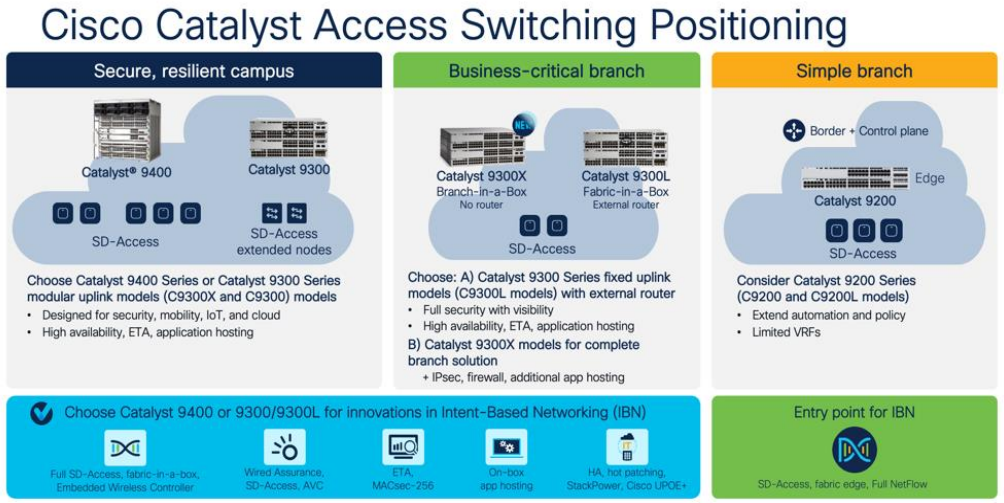
Cisco C9K Architecture Sessions

BRKARC-2098

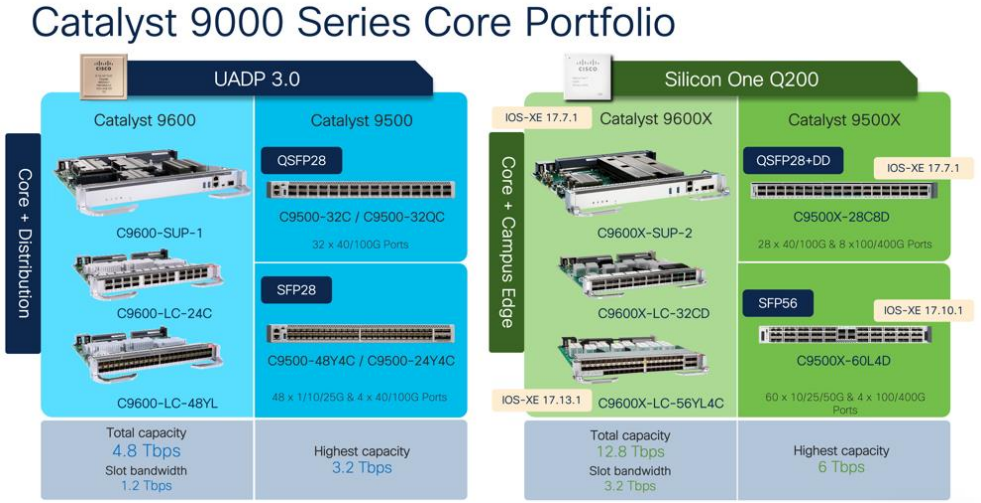
Cisco 9000 Series Switching Family – Access



Includes Cisco C9350 Smart Switches

BRKARC-2099

Cisco 9000 Series Switching Family – Core & Distribution



Includes Cisco C9610 Smart Switches

INTRODUCING

Cisco C9K : the Next Generation of Campus Switching

Cisco Silicon One ASICs, Cloud-native IOS-XE, AI-ready Infrastructure

Silicon One ASICs

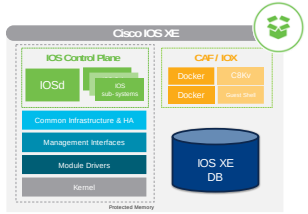
Hardware Adaptability

- Massive Performance for Multi-Gig Access & 100Gig Core
- Massive Campus feature scale (L2/L3, ACL, QoS, NetFlow)
- Embedded PQC Trust Anchor and PQC encryption (MACsec, IPsec)

Multi-Core X86

AI readiness

- Integrated App Hosting for AgenticOps and Firewall agents
- Enhanced Software Services for App Visibility & Network Detection
- Advanced App-Hosting with AI-Hosting (Edge Compute)



Cloud-native IOS XE

Ops & Security

- Built for AI Programmability, Telemetry, Virtualization & Unified Management
- PQC Secure Boot and Live Protect eBPF Compensating Controls
- Zero Downtime architecture with sub-second convergence & upgrade

Sustainable

Smart Power | PoE Assurance | Energy Dashboard

Cisco C9K ASICs & IOS XE Architecture

BRKARC-2092

Cisco C9000 Series Cisco Silicon One and IOS XE Architecture and Innovation

Shawn Wargo - Principal Technical Marketing, Cisco

Key topics covered regarding Cisco ASICs on C9000 Series Switches:

- Why do we need ASICs? (CPUs vs. FPGAs vs. ASICs)
- Cisco UADP and programmable ASICs (the heart of Catalyst 9000 Series Switches)
- An introduction to Cisco SiliconOne ASICs (what's new and different?)
- A glimpse into the future of C9000 Series Switches hardware

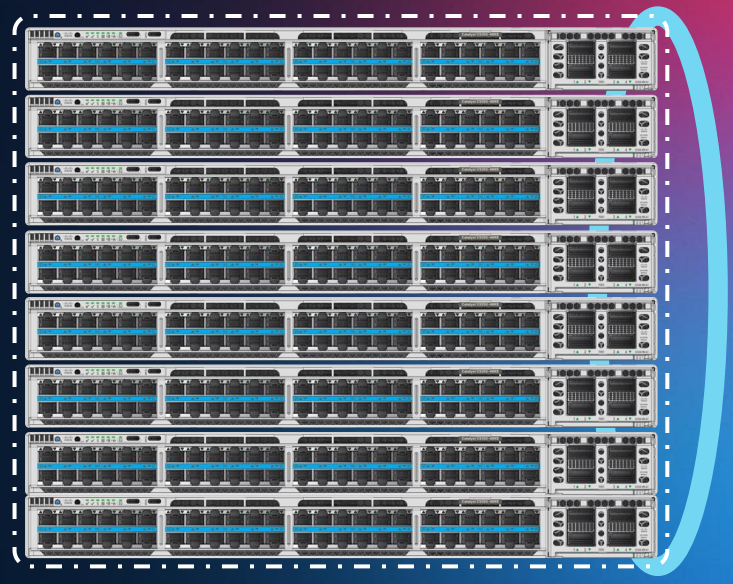
Key topics covered regarding Cisco IOS-XE on C9000 Series Switches:

- Recap of the basic principles and history of Cisco IOS
- Overview of the software components of Catalyst 9000 IOS-XE
- Key innovations enabled by IOS-XE releases 17.9-17.12
- A glimpse into the future of C9000 Series Switches software

This session can be used to help design and position different Cisco C9000 Series switching products - with a deeper understanding of the underlying hardware and software.

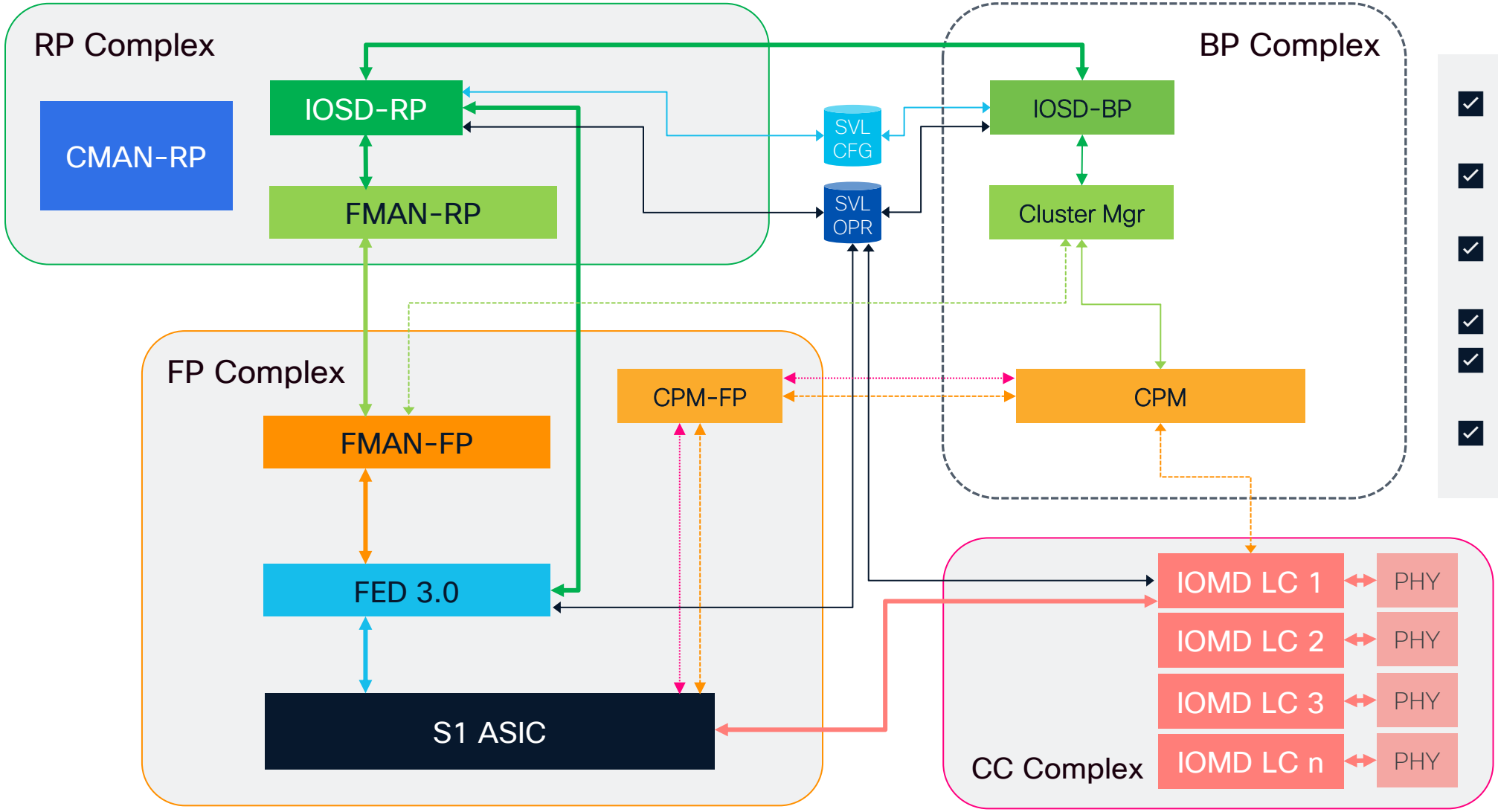
Cisco Smart Stacking

on Cisco C9K Smart Switches



Smart Stacking IOS XE Architecture

REFERENCE



NEW

- IOSd-BP: SVL bringup and management
- Cluster Manager: Node Management
- CPM: Node Discovery & Role Resolution
- LACP: Link Management
- FMAN & CPM-FP: Data-Plane Management
- FED 3.0 & SDK: Hardware Abstraction:

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Bootstrap Process & Cluster Manager

REFERENCE

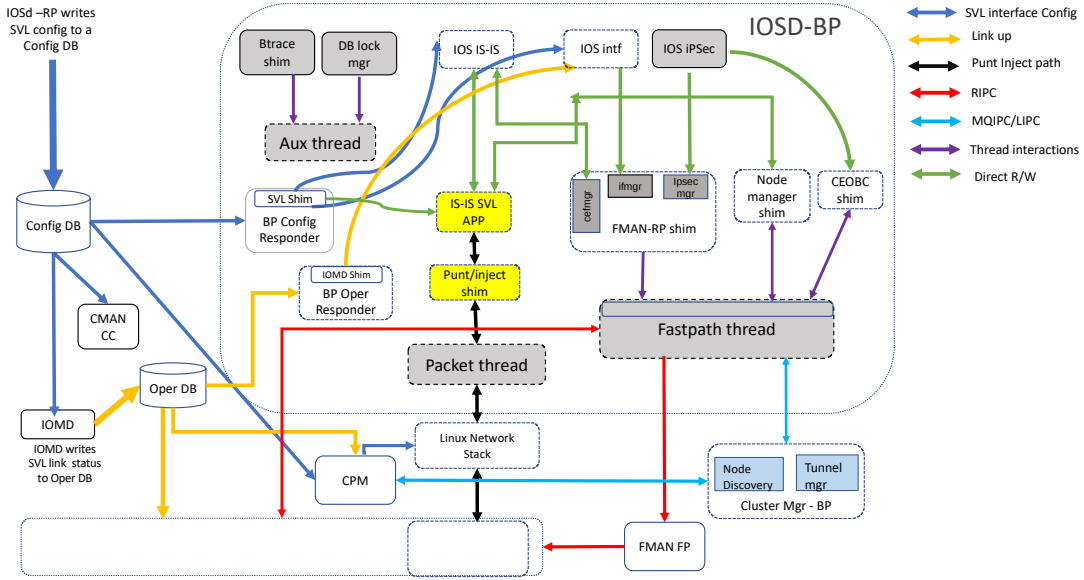
Cisco IOS-XE introduces a new virtual Bootstrap Plane (BP) complex - in addition to the current RP, FP & CC complexes

An IOSd process to bootstrap SVL interfaces (IOSd-BP) and Cluster Platform Manager (CPM) run in the new BP complex.

IOSd-BP handles the Cluster-Manager process and SPF (IS-IS) process to establish a Cluster 'Ethernet Out-of-Band Channel' (virtual backplane) tunnel and discover other SVL nodes.

IOSd-BP & CPM tasks:

1. Starts before IOSd-RP during bootup & parses any SVL interface config
2. Creates an IS-IS process for discovering internal nodes
3. Create and download SVL interfaces to FMAN and dataplane
4. Interreact with IOMD for SVL interface and port events
5. IS-IS process in IOSd-BP will do SVL node discovery
6. Cluster EOBC is opened through IOSd-BP
7. Downloads FMAN objects to FMAN-FP via MQIPC link
8. SVL nodes join/leave later will be discovered by IS-IS in IOSd-BP



IOSd-BP & CPM run as a separate Linux thread

VXLAN-GPE Stack Encapsulation

REFERENCE

Smart Stacking (NG-SVL) uses a standard 64B VXLAN-GPE header with Next Protocol: Switch ID & Port ID information

- The outermost header fields are standard Ethernet (MAC), IP and UDP headers.
- VXLAN-GPE header includes a new Next Protocol field to carry additional protocol information.
- Stack members insert the Switch ID and Port ID information (and other metadata, e.g. QoS, Multicast, etc.) to be used by IOSd-BP and CPM (IS-IS).

IETF | Internet Engineering Task Force
https://www.ietf.org › draft-ietf-nvo3-vxlan-gpe-12

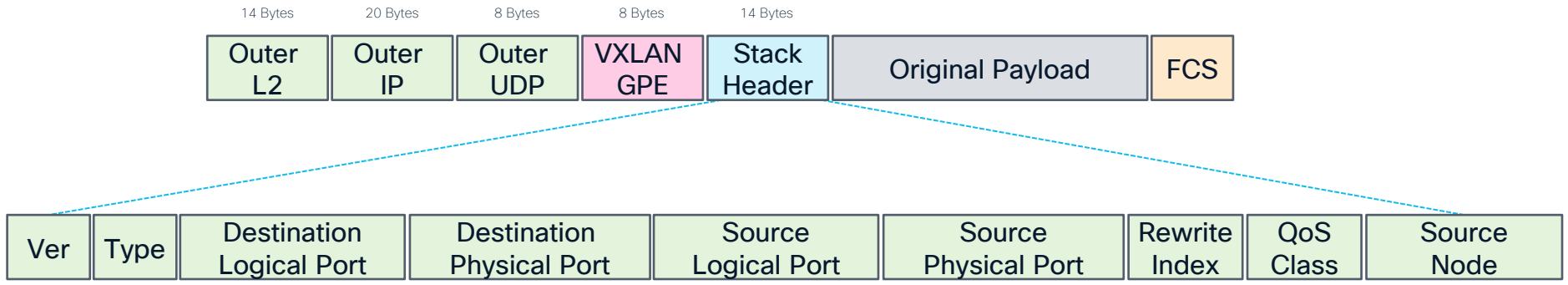
Generic Protocol Extension for VXLAN (VXLAN-GPE)

3. Generic Protocol Extension for VXLAN (VXLAN-GPE)

3.1. VXLAN-GPE Header

```
 0                   1                   2                   3
 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|R|R|Ver|I|P|B|O|       Reserved                |Next Protocol  |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|                VXLAN Network Identifier (VNI) |   Reserved    |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

Figure 2: VXLAN-GPE Header



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Cisco Smart Stacking

C9350 Smart Stacking

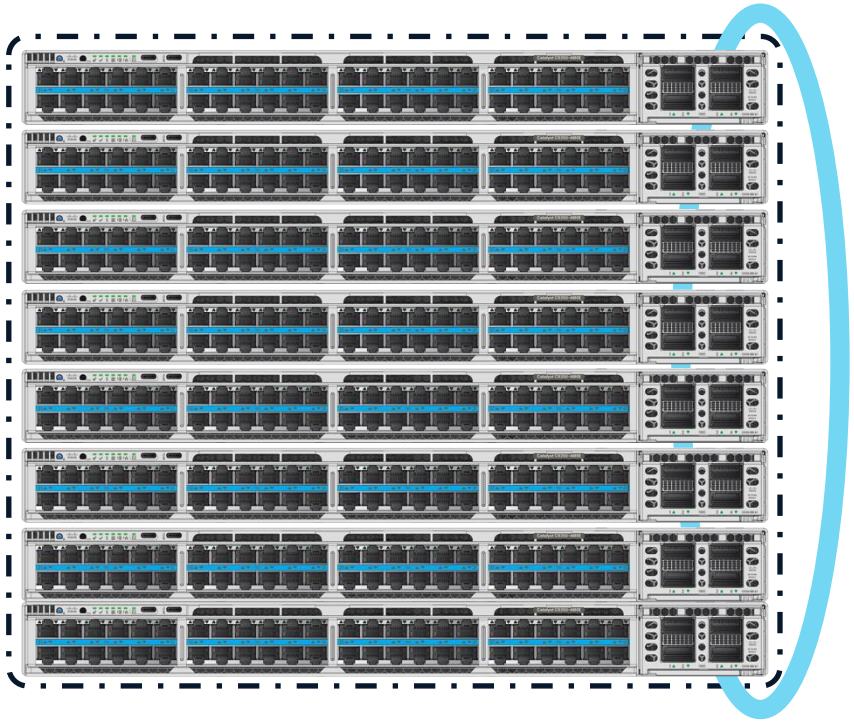
on C9350 Smart Switches

CISCO Live !

Cisco C9350 Series Switches

New stacking architecture for the new generation of campus access

Redesigned stacking architecture from the ground-up for the new generation of access switches.



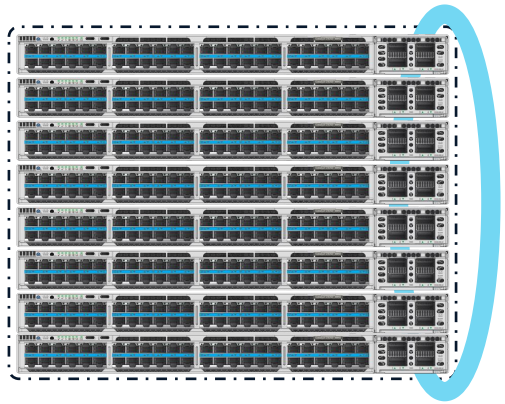
- NEW 1.6T Guaranteed Stacking bandwidth
- NEW User friendly Point to Point Stacking design
- NEW Isolated bandwidth loss in event of failure
- NEW Enhanced Stackpower: more power draw per cable

Cisco C9350 Smart Stacking (NG-SVL)

New architecture for the new networking demands

1

New point-to-point stacking architecture

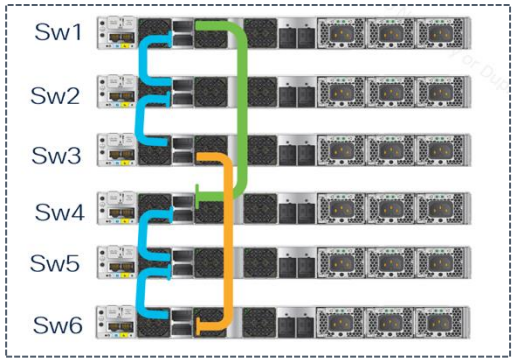


Uses standards-based Shortest Path First algorithm

Same code as front-panel stacking

2

Flexible user-friendly stacking design

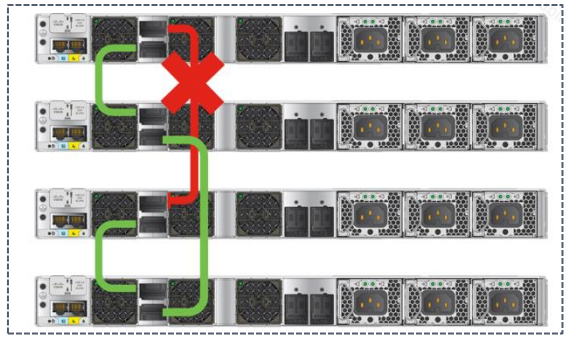


No restrictions on how or where you connect to form a full ring.

Eliminate long cable requirement

3

Isolated bandwidth loss during failure

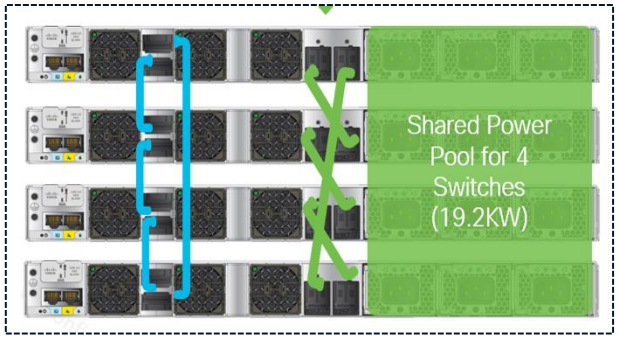


Failure only affects bandwidth for directly connected switches.

Remains operating at full bandwidth

4

Enhanced StackPower Higher power sharing



New cables handle higher current (55A)

30% more power sharing

Unique to the C9350 series (Not applicable for C9300/L/X series)

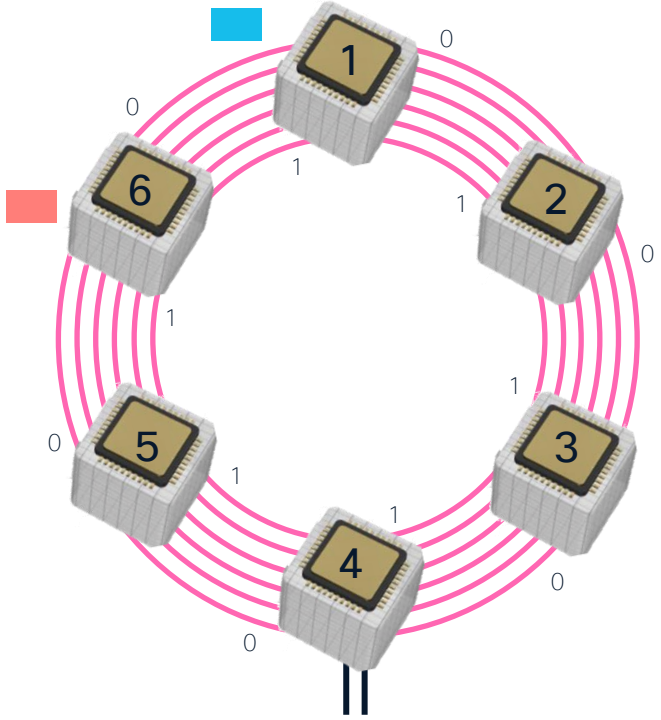
SPF Forwarding for Access Stacking

Example: 6-member Access Stack

Sw1 Port0- Sw4 Port0
Sw1 Port1- Sw2 Port0
Sw2 Port1- Sw3 Port0
Sw3 Port1- Sw6 Port1
Sw4 Port1- Sw5 Port0
Sw5 Port1- Sw6 Port0

Current Cisco StackWise

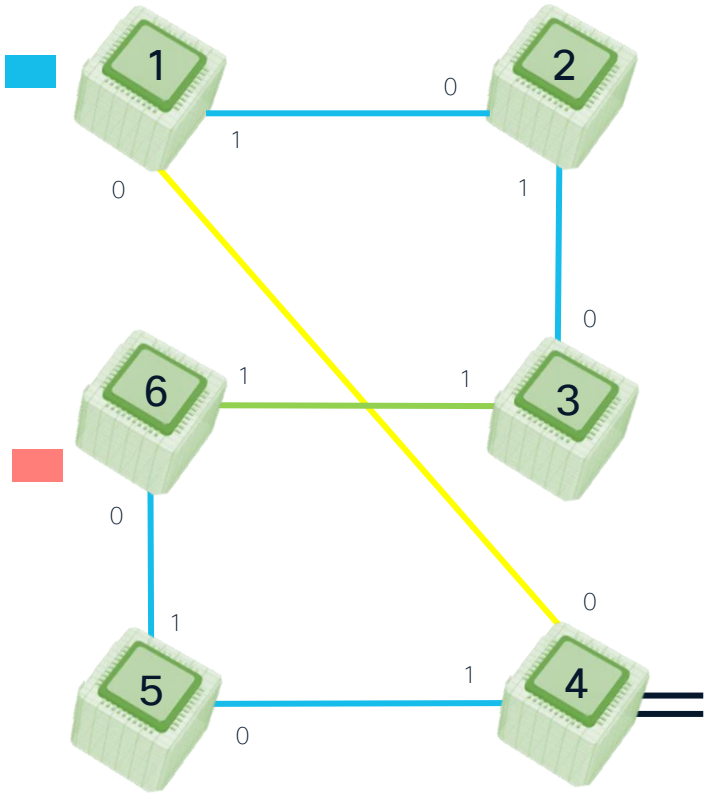
Ring-based stacking



- Inflexible Ring Cabling Configuration
- Spatial Re-Use Algorithm
- Shared Best Effort Bandwidth

Cisco Smart Stacking (NG-SVL)

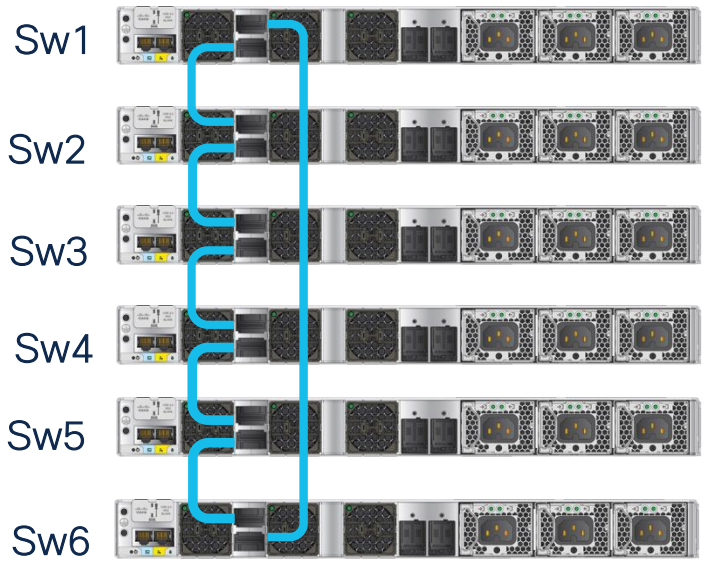
SPF-based stacking



- Flexible Mesh Cabling Design
- Proven L3 SPF ECMP Algorithm
- Low Latency and Guaranteed Bandwidth

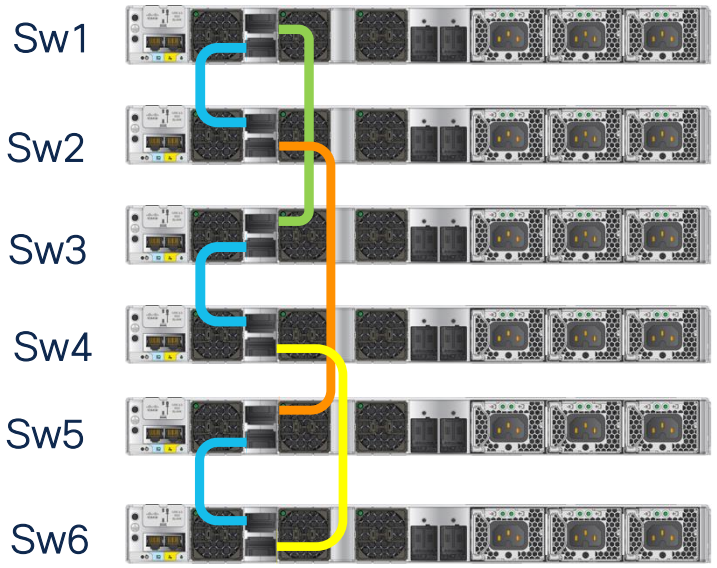
Ensures minimal latency , high throughput and consistent forwarding

C9350 Smart Stacking – Cable configuration options

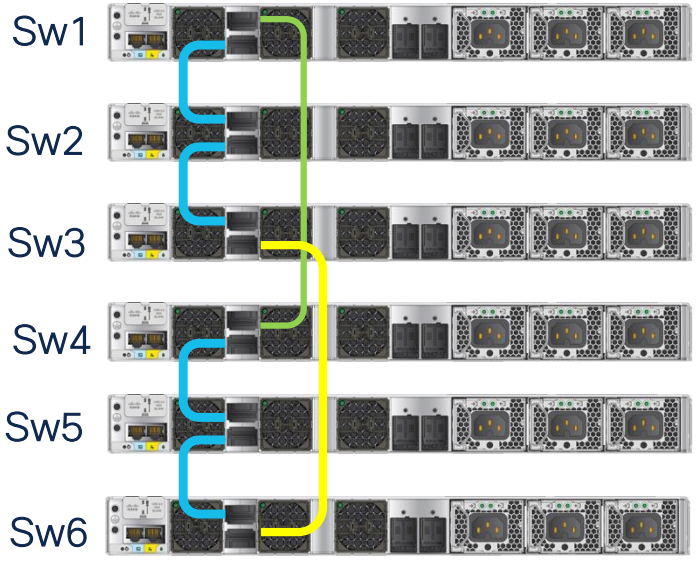


Typical Stack Cables Configurations

Sw1 Port1 – Sw2 Port0
Sw2 Port1 – Sw3 Port0
Sw3 Port1 – Sw4 Port0
Sw4 Port1 – Sw5 Port0
Sw5 Port1 – Sw6 Port0
Sw6 Port1 – Sw1 Port0



Sw1 Port0 – Sw3 Port0
Sw1 Port1 – Sw2 Port0
Sw2 Port1 – Sw5 Port0
Sw3 Port1 – Sw4 Port0
Sw4 Port1 – Sw6 Port1
Sw5 Port1 – Sw6 Port0



Sw1 Port0 – Sw4 Port0
Sw1 Port1 – Sw2 Port0
Sw2 Port1 – Sw3 Port0
Sw3 Port1 – Sw6 Port1
Sw4 Port1 – Sw5 Port0
Sw5 Port1 – Sw6 Port0

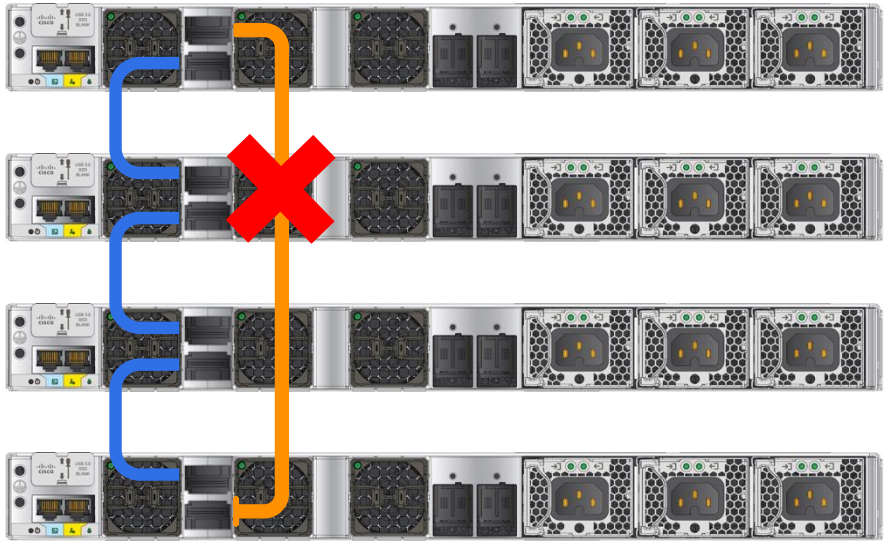
As stack grows – it provides greater flexibility in connecting cables in different configurations with shorter stack cables. No restrictions on how or where you connect to form a full ring.

Considering 6 x C9350 Switches in Stack

C9350 Smart Stacking – Enhanced stacking resiliency

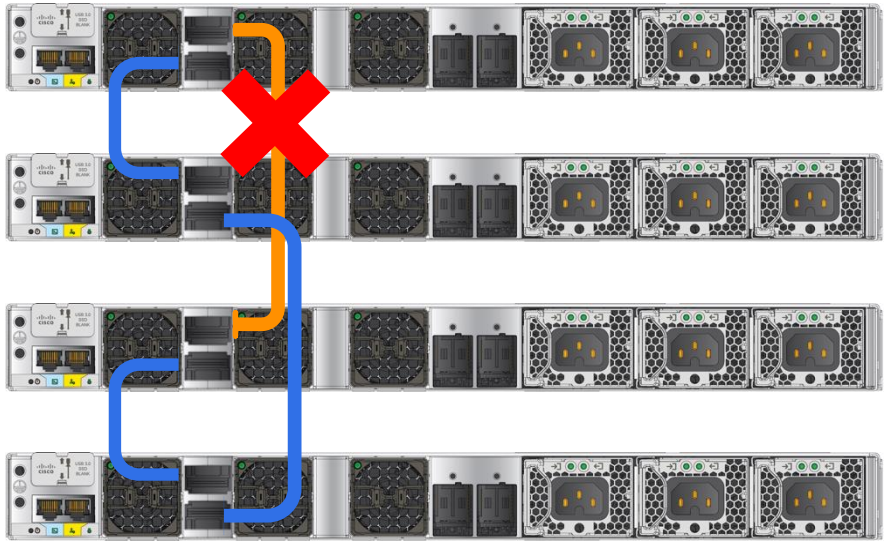
Stack Link Failure Handling

Current Cisco StackWise



A single failure effectively
halves bandwidth for the entire stack

Cisco Smart Stacking (NG-SVL)



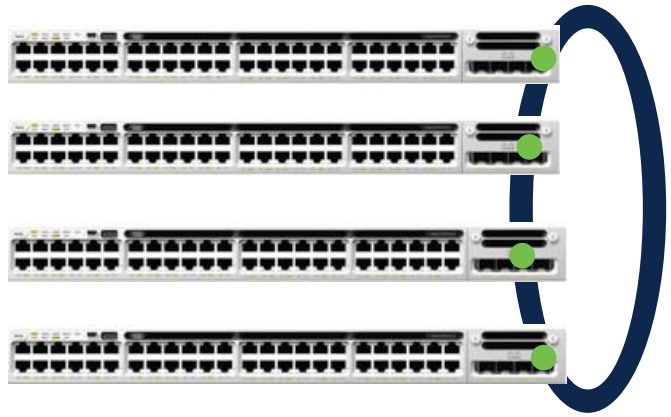
Switch 1 to 3 bandwidth is halved.
Other switches operate at full bandwidth

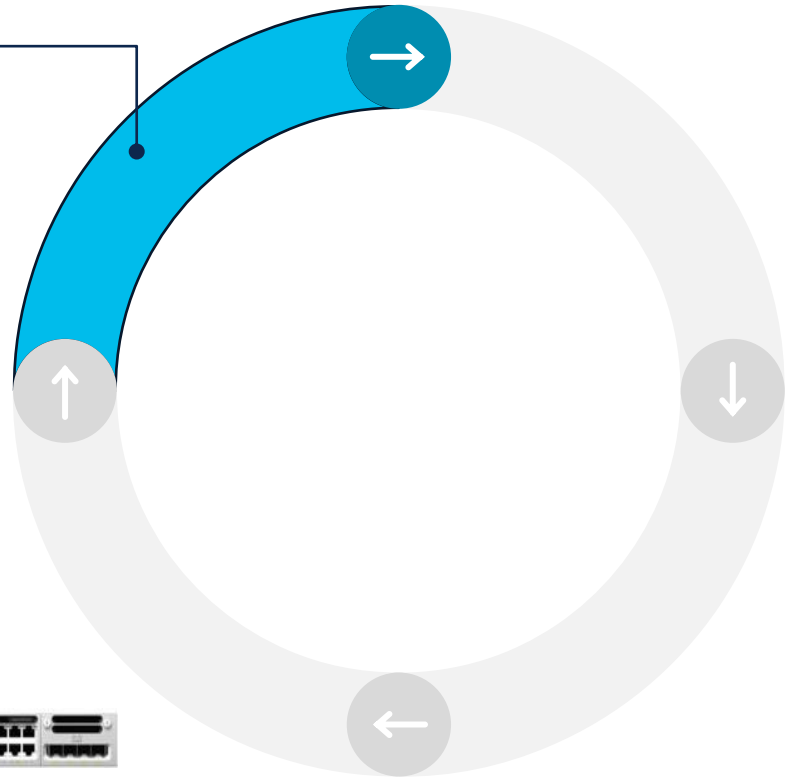
```
C9350# show switch stack-bandwidth
                          Stack        Current
C9350#   Role           Bandwidth    State
-----------------------------------------
*1       Active          800G        Ready
 2       Standby        1600G        Ready
 3       Member          800G        Ready
 4       Member         1600G        Ready
```

A link failure only affects bandwidth for directly connected switches – all other switches operate at full bandwidth

Stacking process – Stack discovery

Stack Discovery via standard Ethernet Protocol (ISIS)





Stack interfaces brought online

ISIS Protocol runs

Ring: Discovery exits after all members are found

Other Topology: System waits for 6 seconds

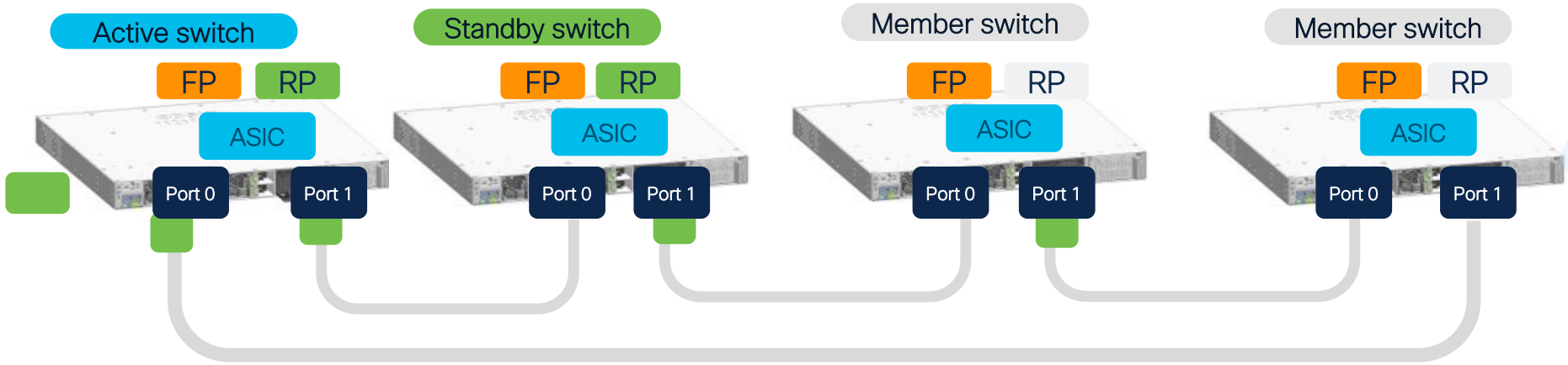
Stack Neighbor Discovery

Stack interface are brought online - Enables ISIS protocols → Link Local Packets are sent to bring up ISIS adjacency → Once UP Adjacency is sent to Cluster Manager (coordinates multiple switches in stack) → Cluster Manager sends ISIS GenInfo TLV for role Resolution

Rapid Ring Discovery algorithm ensure faster discovery in Half/Full Ring topologies

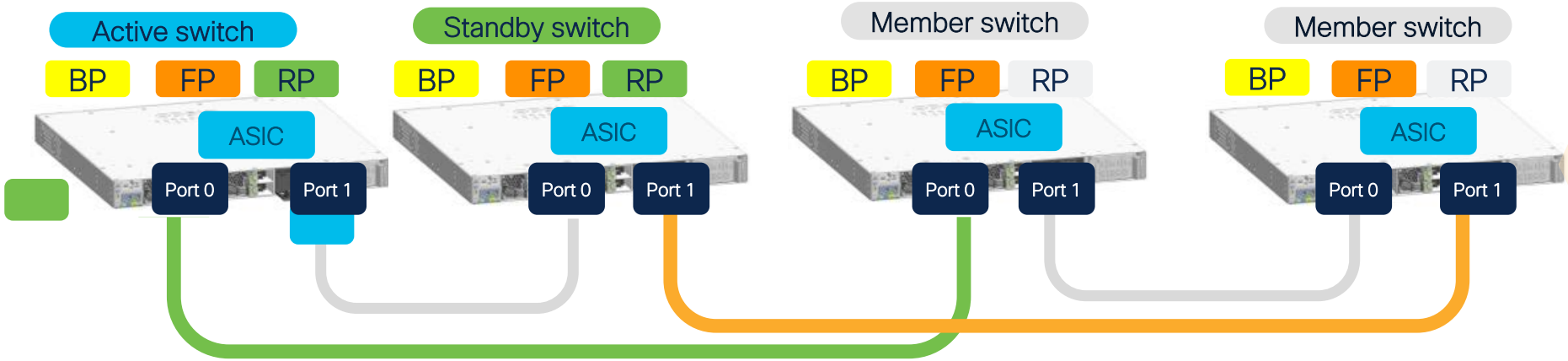
C9350 Smart Stacking

Forwarding behaviour comparison



Traditional Ring Stacking Architecture

Each packet is fragmented and load-balanced across ports, and reassembled at the destination.



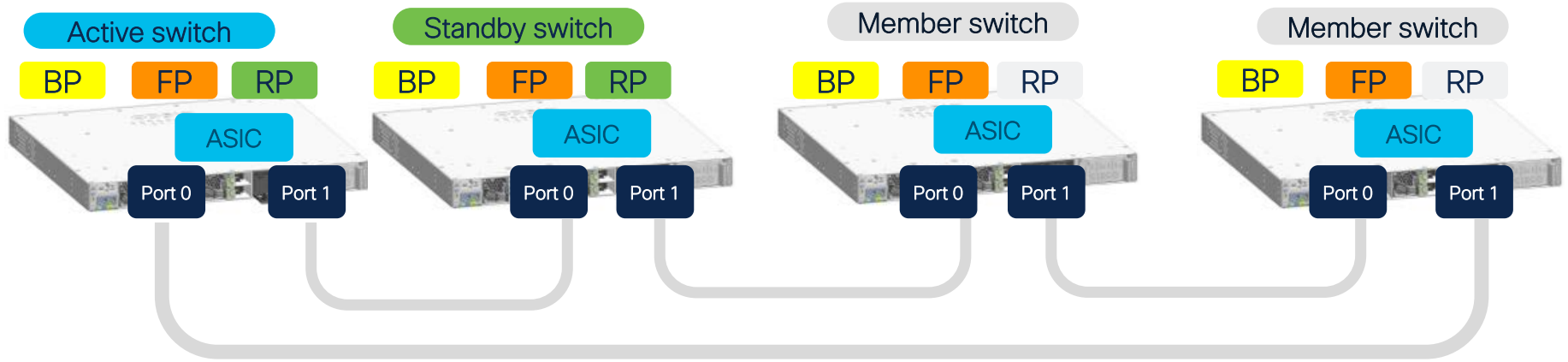
New SPF-based Stacking Architecture

Each Packet is transmitted complete, unfragmented, across point-to-point links

Cisco C9350 Series Smart Switch

Stacking Packet Walk

Consider Source port on Switch 1 with Destination on Switch 3



1 **Packet Received on Switch 1**

2 **Rx-NPU (Ingress Processing) on Switch 1:**

- Adds **NPU header** (for processing by TxNPU at egress).
- Adds **TM header** (for traffic management at egress).
- Adds **Stack header** (to ensure packet forwarding across stack).

3 **Tx-NPU (Egress Processing) on Switch 1:**

- Identifies **Switch 3 as the destination**.
- Encapsulates the packet with necessary VXLAN stack headers.
- Sends the packet to the next switch in the stack ring.

4 **Intermediate Hop :**

- **Rx-NPU on intermediate switch** processes the stack header.
- Recognizes **Switch 3 as the final destination**.
- Forwards the packet to Switch 3 through the stack NPU.

5 **Rx-NPU (Ingress Processing) on Switch 3:**

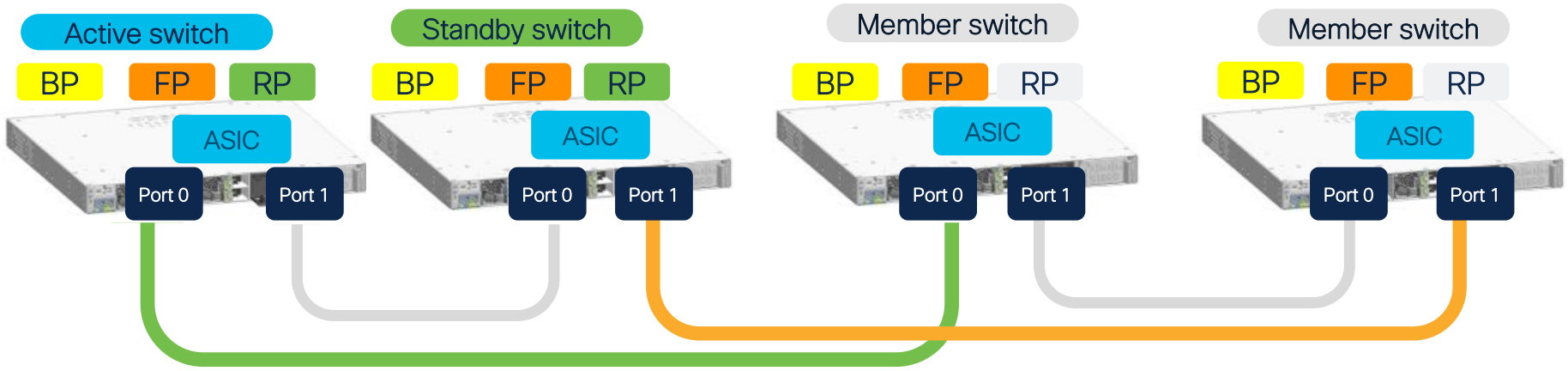
- Looks at stack header and forward to TM/TXNPU

6 **Tx-NPU/TM on Switch 3:**

- Decapsulates stack, TM, and NPU headers.
- Processes **traffic manager PD** for forwarding decision.
- Determines the correct **egress port**.

Cisco C9350 Series Smart Switch

Equal Cost Multiple Path Load-Balancing



Stack traffic can either be load-balanced across two ports or follow a Shortest Path First (SPF)

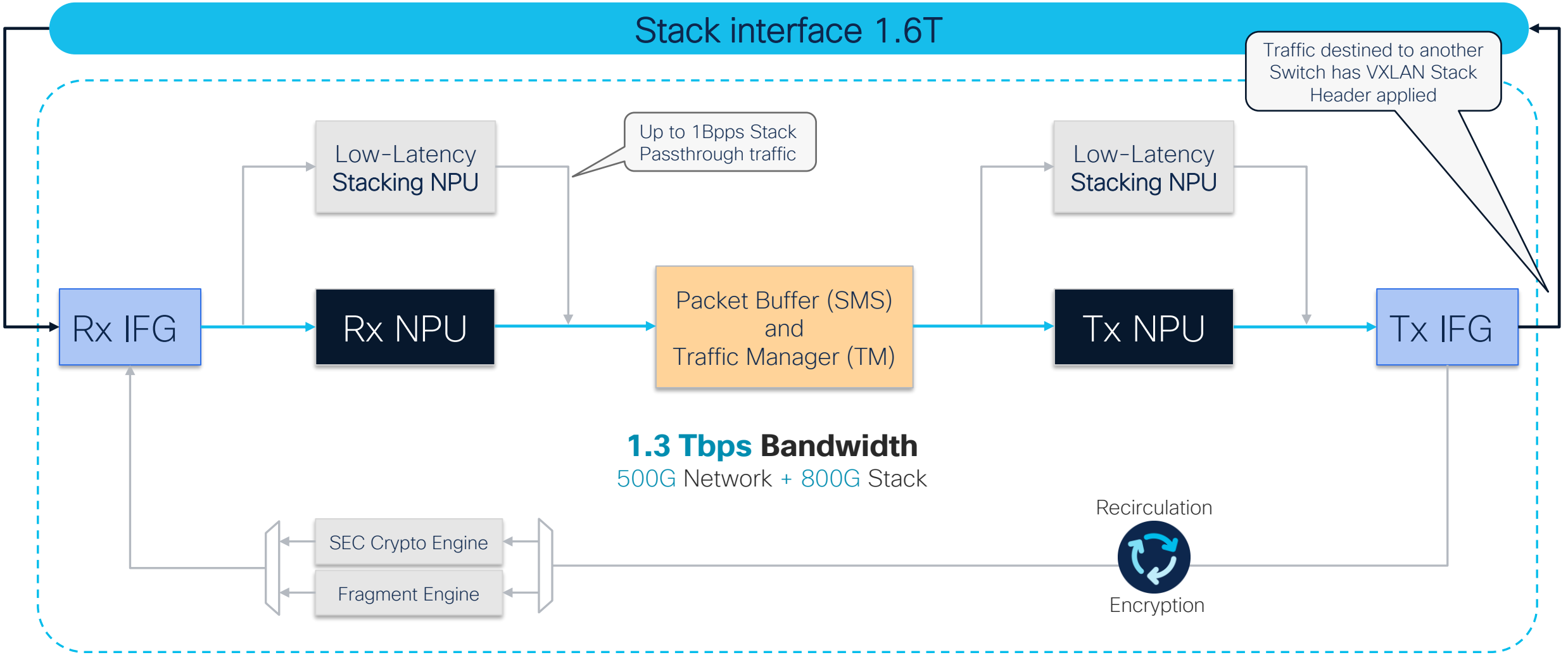
Consider **Source** on **Switch 1** with **Destination** on **Switch 3**

The new architecture can leverage the shortest direct path for optimal traffic flow.
The path is computed based on Source/Destination and other parameters evaluated by the Algorithm automatically.

Ensures minimal latency, high throughput and consistent packet forwarding

Cisco C9350 Series with S1 A100 ASIC

Specialized Stacking hardware architecture

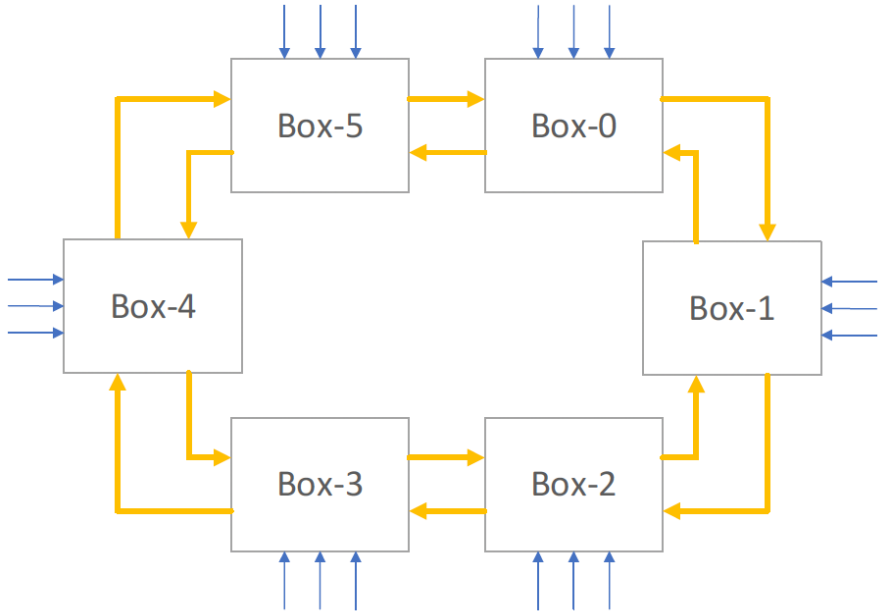


C9350 Smart Stacking - Stack Ports

REFERENCE

Logical Stack Ports

- 2x 800Gbps (1.6 Tbps) bidirectional bandwidth
- Up to four 200G (MAC) ports
  - 2x Stack Ports (0 [Top] & 1 [Bottom])
  - 2x ASIC Ports (for Multi-ASIC models)

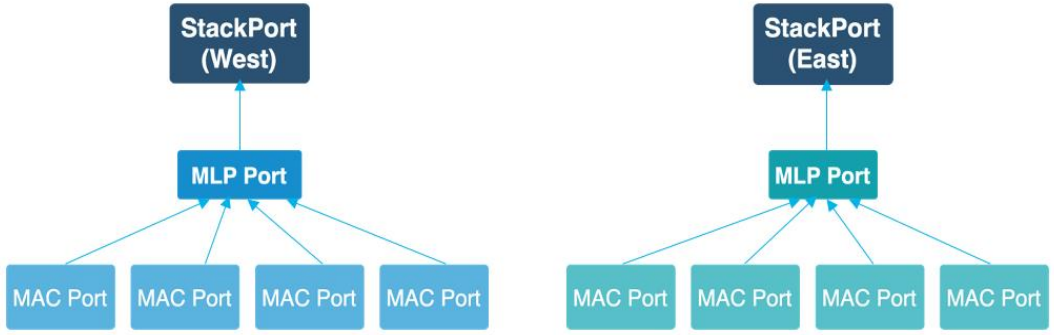


Stack Port Load Balancing

- East/West path selection on Stack
- Load balancing: ECMP or weighted ECMP

Multi-Link Port Load Balancing

- Bundled up to 4 same-speed links
- Packet-by-packet load balancing
- Sequence number-based reordering



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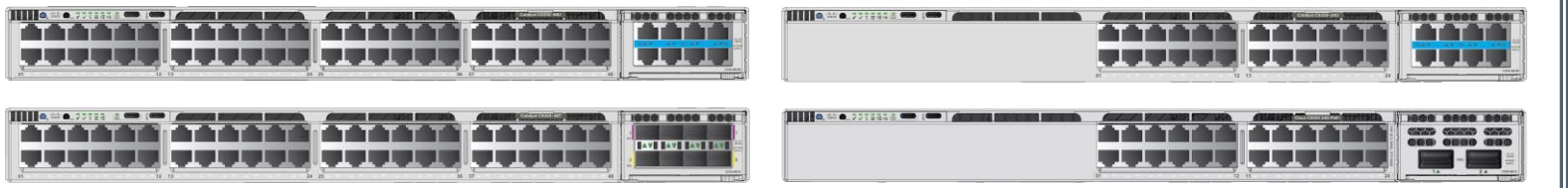
C9350 Smart Stacking - Stack Port port mapping

REFERENCE

Stack Port	Etherchannel	C9350-48U/P/T	C9350-24U/P/T	C9350-HX/TX
Top Port (External)	**Po241**	**49 to 52** (ASIC-0)	**25 to 28** (ASIC-0)	**49 to 52** (ASIC-1)
Bottom Port (External)	**Po242**	**53 to 56** (ASIC-0)	**29 to 32** (ASIC-0)	**53 to 58** (ASIC-0)
ASIC Port -1 (Internal)	**Po243**	NA	NA	**57 to 60** (ASIC-1)
ASIC Port -2 (Internal)	**Po244**	NA	NA	**61 to 64** (ASIC-0)



Single ASIC - 9350 U/P/T

Dual ASIC - 9350 HX/TX

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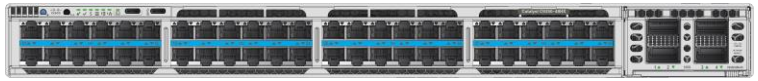
C9350 Smart Stacking – Stack Port interface numbering

REFERENCE

Stack interfaces: 100G ports numbered by Switch, Bay 0, Port

CLI : "*show platform software fed switch <sw#> ifm mapping*"

Output Captured from Switch 1 – Dual ASIC 48 port Switch



```
C9350# show platform software fed switch 1 ifm mapping
Interface                IF_ID  Inst Asic Core IFG_ID Port SubPort Mac  First Serdes Last Serdes  Cntx LPN  GPN   Type Active
C9350# show platform software fed switch 1 ifm mapping | in HundredGigE1/0/
HundredGigE1/0/49        0x35     1    1    0      0    0       0    49   8            9            0    49   49    NIF    Y
HundredGigE1/0/50        0x38     1    1    0      0    0       0    50   10           11           0    50   50    NIF    Y
HundredGigE1/0/51        0x39     1    1    0      0    0       0    51   12           13           0    51   51    NIF    Y
HundredGigE1/0/52        0x3a     1    1    0      0    0       0    52   14           15           0    52   52    NIF    Y
HundredGigE1/0/53        0x3b     0    0    0      0    0       0    53   0            1            0    53   53    NIF    Y
HundredGigE1/0/54        0x3d     0    0    0      0    0       0    54   2            3            0    54   54    NIF    Y
HundredGigE1/0/55        0x3e     0    0    0      0    0       0    55   4            5            0    55   55    NIF    Y
HundredGigE1/0/56        0x3f     0    0    0      0    0       0    56   6            7            0    56   56    NIF    Y
HundredGigE1/0/57        0x40     1    1    0      0    0       0    57   6            7            0    57   57    NIF    Y
HundredGigE1/0/58        0x42     1    1    0      0    0       0    58   4            5            0    58   58    NIF    Y
HundredGigE1/0/59        0x43     1    1    0      0    0       0    59   2            3            0    59   59    NIF    Y
HundredGigE1/0/60        0x44     1    1    0      0    0       0    60   0            1            0    60   60    NIF    Y
HundredGigE1/0/61        0x45     0    0    0      0    0       0    61   8            9            0    61   61    NIF    Y
HundredGigE1/0/62        0x47     0    0    0      0    0       0    62   10           11           0    62   62    NIF    Y
HundredGigE1/0/63        0x48     0    0    0      0    0       0    63   12           13           0    63   63    NIF    Y
HundredGigE1/0/64        0x49     0    0    0      0    0       0    64   14           15           0    64   64    NIF    Y
C9350#
```

Top External EAST

Bottom External WEST

ASIC Internal WEST

ASIC Internal EAST

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C9350 Smart Stacking – Show Switch CLIs


```
C9350# show switch
Switch/Stack Mac Address : 9ca9.b82b.5480 - Local Mac Address
Mac persistency wait time: Indefinite
                                                     H/W   Current
Switch#   Role    Mac Address     Priority Version  State
------------------------------------------------------------------------
*1       Active   9ca9.b82b.5480     13      P1      Ready
 2       Standby  40f4.9f46.8d80     12      P1      Ready
 3       Member   9ca9.b82b.3a80     11      P1      Ready
 4       Member   40f4.9f46.8400     7       P1      Ready
 5       Member   28b5.917d.b000     5       P1      Ready
 6       Member   9ca9.b82b.4400     3       P1      Ready
 7       Member   9ca9.b82b.2f80     2       P1      Ready
 8       Member   9ca9.b82b.5180     1       P1      Ready

C9350#
```

```
C9350# show switch stack-port summary
Sw#/Port#  Port Status  Neighbor/Port  Cable Length   Link OK   Link Active   Sync OK   #Changes to LinkOK  In Loopback
-------------------------------------------------------------------------------------------------------------------
1/1        OK           8/2            50cm           Yes       Yes           Yes       0                   No
1/2        OK           2/1            100cm          Yes       Yes           Yes       0                   No
2/1        OK           1/2            100cm          Yes       Yes           Yes       0                   No
2/2        OK           3/1            300cm          Yes       Yes           Yes       0                   No
3/1        OK           2/2            300cm          Yes       Yes           Yes       0                   No
3/2        OK           4/1            300cm          Yes       Yes           Yes       0                   No
4/1        OK           3/2            300cm          Yes       Yes           Yes       0                   No
4/2        OK           5/2            50cm           Yes       Yes           Yes       0                   No
5/1        OK           6/1            50cm           Yes       Yes           Yes       0                   No
5/2        OK           4/2            50cm           Yes       Yes           Yes       0                   No
6/1        OK           5/1            50cm           Yes       Yes           Yes       0                   No
6/2        OK           7/1            50cm           Yes       Yes           Yes       0                   No
7/1        OK           6/2            50cm           Yes       Yes           Yes       0                   No
7/2        OK           8/1            50cm           Yes       Yes           Yes       0                   No
8/1        OK           7/2            50cm           Yes       Yes           Yes       0                   No
8/2        OK           1/1            50cm           Yes       Yes           Yes       0                   No

C9350#
```

C9350 Smart Stacking – Show Switch CLIs

REFERENCE

```
C9350# show switch stack-bandwidth
                    Stack          Current
Switch#   Role      Bandwidth      State
-----------------------------------------
*1        Active    1600G          Ready
 2        Standby   1600G          Ready
 3        Member    1600G          Ready
 4        Member    1600G          Ready
 5        Member    1600G          Ready
 6        Member    1600G          Ready
 7        Member    1600G          Ready
 8        Member    1600G          Ready

Switch#
```

```
Switch# show switch stack-mode
Switch#  Role    Mac Address     Version   Mode  Configured  State
-------------------------------------------------------------------
*1       Active  9ca9.b82b.5480    P1      N+1     None       Ready
 2       Standby 40f4.9f46.8d80    P1      N+1     None       Ready
 3       Member  9ca9.b82b.3a80    P1      N+1     None       Ready
 4       Member  40f4.9f46.8400    P1      N+1     None       Ready
 5       Member  28b5.917d.b000    P1      N+1     None       Ready
 6       Member  9ca9.b82b.4400    P1      N+1     None       Ready
 7       Member  9ca9.b82b.2f80    P1      N+1     None       Ready
 8       Member  9ca9.b82b.5180    P1      N+1     None       Ready


C9350#
```

```
C9350# show switch stack-ring speed

Stack Ring Speed          : 1600G
Stack Ring Configuration: Full
Stack Ring Protocol       : StackWise


C9350#
```

```
C9350# show switch neighbors
  Switch #    Port 1       Port 2
  --------    ------       ------
      1          8            2
      2          1            3
      3          2            4
      4          3            5
      5          6            4
      6          5            7
      7          6            8
      8          7            1

C9350#
```


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Cisco Smart Stacking

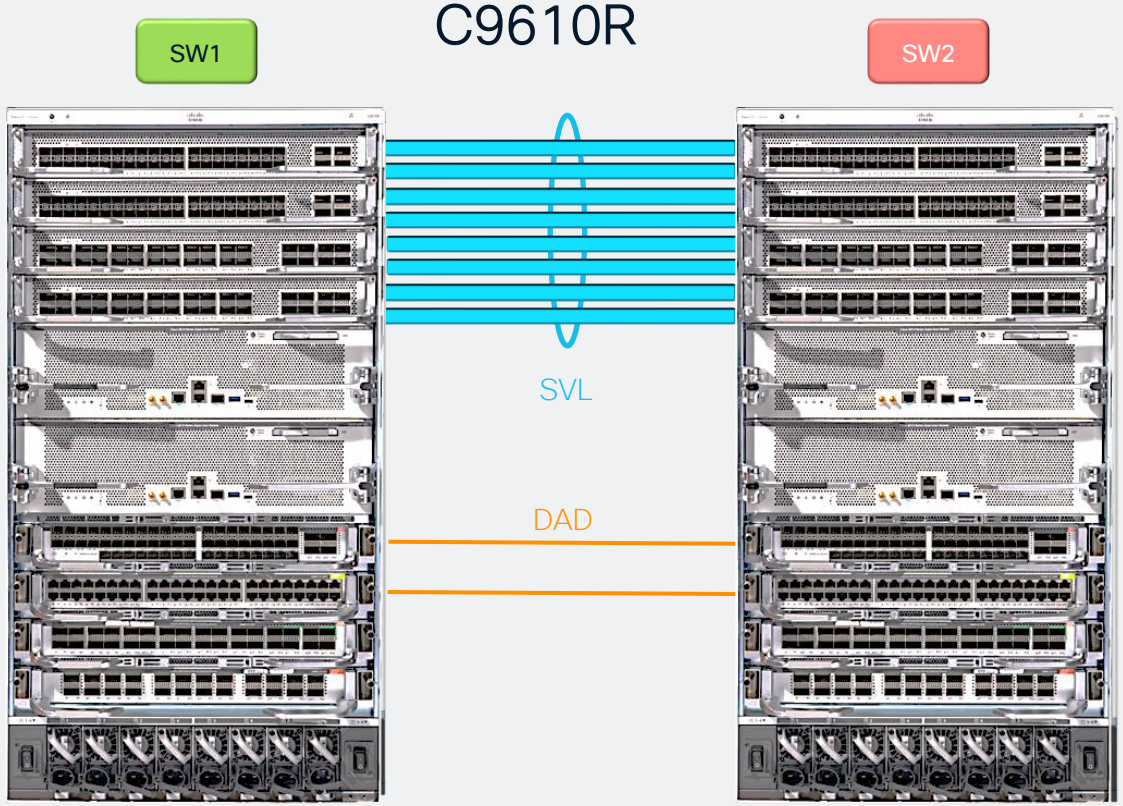
C9610 Smart Stacking

on C9610 Smart Switches

CISCO Live !

Cisco C9610 Smart Stacking (NG-SVL)

17.18.2



Standard Ethernet-based SVL

- IS-IS Shortest-Path-First (SPF) Forwarding
- VXLAN Ethernet SVL Header Encapsulation

Support C9610-SUP-3 or 3XL

- Supervisor models must match

Support up to 16 Line-Cards

- SVL support on any ports
- Up to 8 x 100G (800G)
- Up to 8 x 400G (1.6T)

Dynamically Add & Remove Links

- SVL ports
- DAD ports

TIP Back-panel (C9350) and front-panel (C9610) stacking use the **same implementation**

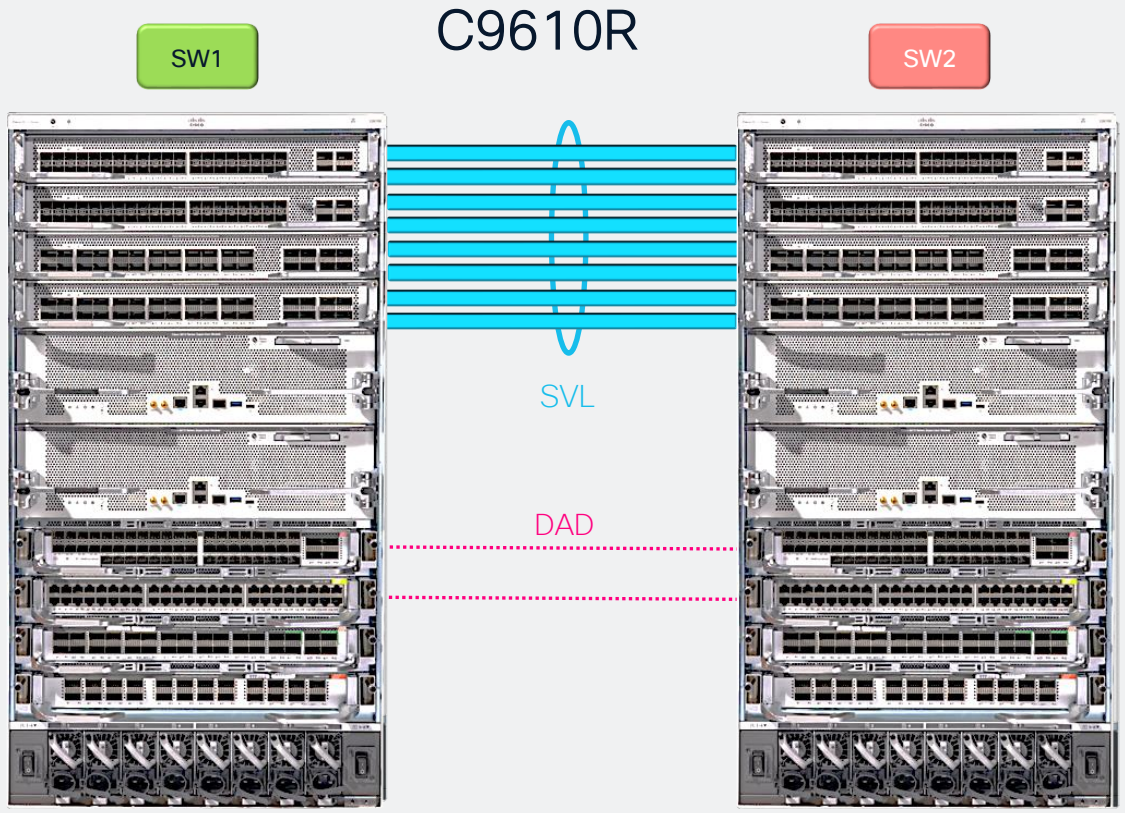
Cisco C9610 Smart Stacking (NG-SVL)

17.18.2

Consistent with existing C9600 SVL

SVL: StackWise Virtual Link
- Up to 8 ports (Portchannel)
  - 10/25 & 50G SFP
  - 40/100 & 400G QSFP
- Same speed for all SVL links
- Distribute across Line-Cards

DAD: Dual Active Detection
- Fast Hello
  - Directly-connected
  - Up to 4 links
  - 1/10G RJ45 or SFP
- Enhanced PAgP
  - PAgP EtherChannel
  - Up to 4 channels



In SVL mode: 2nd Supervisor in chassis (ICS) is currently not supported and will be powered off

Dynamic Add & Removal of Stack Links

17.18.2

C9610 Smart Stacking supports dynamic addition and removal of external SVL and DAD Links.

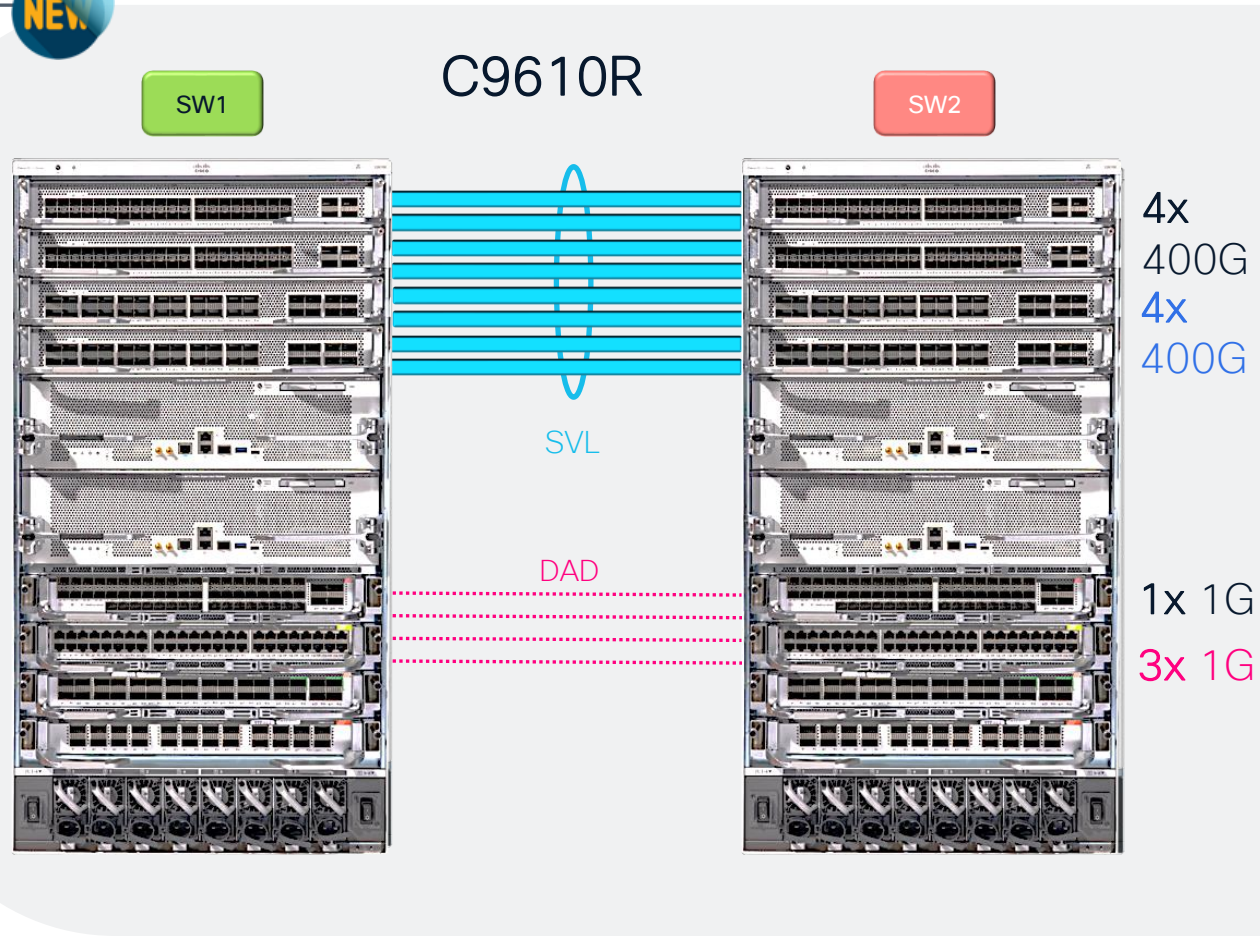
NEW

Flexible Add or Remove links whenever required

In an integrated Multi-ASIC + Fabric system, any update to SVL or DAD links results in re-election of the Control link, which needs to consider the ASIC 0 associated SVL path to be chosen as next Control link.

FED and CPM software components will be updated with the new control link selection algorithm to ensure the best control link possible. SVL Control link change also results in moving all SVL SPF (IS-IS) and SVL IPC traffic to be redirected to the newly elected link.

This is handled in a Multi-ASIC environment by updating all the K100 ASICs within the chassis to reflect the correct new CPU (Punt and Inject) destination port, avoiding broken peer reachability or stack split scenario.



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C9610 Smart Stacking – Show SVL CLIs

REFERENCE

```
switch# show switch
Switch/Stack Mac Address : 40b5.c1ff.c600 - Local Mac Address
Mac persistency wait time: Indefinite
                                             H/W   Current
Switch#   Role    Mac Address     Priority Version  State
------------------------------------------------------------
*1       Active   40b5.c1ff.c600     1      V02     Ready
 2       Standby  f87a.4137.c600     1      V02     Ready
```

```
C9610# show redundancy state
       my state = 13 -ACTIVE
     peer state = 8  -STANDBY HOT
           Mode = Duplex
           Unit = Primary
        Unit ID = 1

Redundancy Mode (Operational) = sso
Redundancy Mode (Configured)  = sso
Redundancy State              = sso
     Maintenance Mode = Disabled
    Manual Swact = enabled
 Communications = Up
```

```
C9610# show stackwise-virtual link
Stackwise Virtual Link(SVL) Information:
----------------------------------------
Flags:
------
Link Status
-----------
U-Up D-Down
Protocol Status
---------------
s-Suspended P-Bundled E-Error D-Down R-RLayer3 I-Indiv
-----------------------------------------------------
Switch  SVL     Ports                          Link-Status     Protocol-Status
------  ---     -----                          -----------     ---------------
1       1       HundredGigE1/0/6               U               P
                HundredGigE1/0/7               U               P
2       1       HundredGigE2/0/6               D               P
                HundredGigE2/0/7               U               P

Switch# show stackwise-virtual dual-active-detection
In dual-active recovery mode: No
Recovery Reload: Enabled

Dual-Active-Detection Configuration:
------------------------------------
Switch  Dad port                       Status
------  ------------                   ---------
1       HundredGigE1/0/1               up
        HundredGigE1/0/2               up
2       HundredGigE2/0/1               up
        HundredGigE2/0/2               up
```


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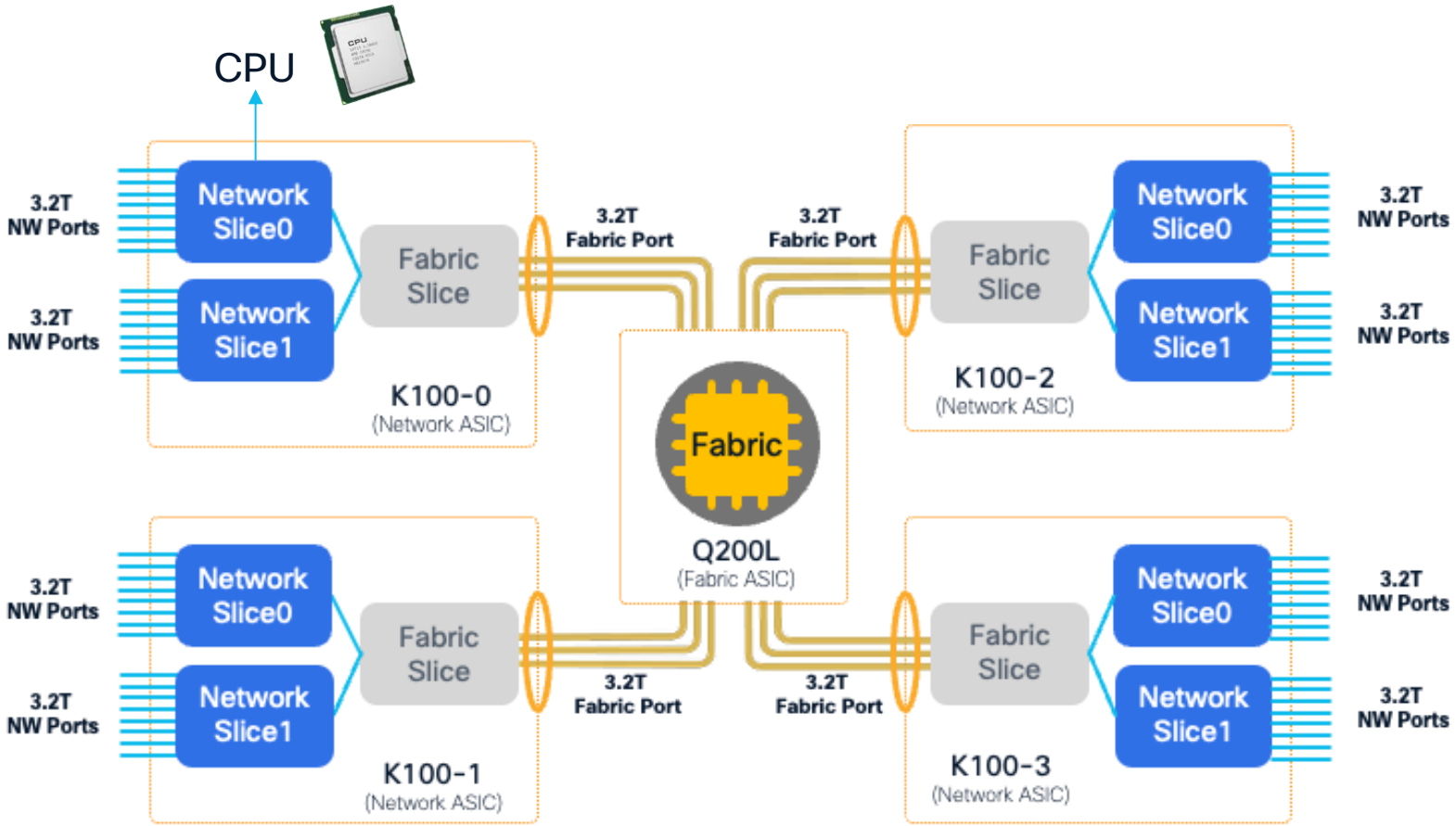
Cisco C9610 Series with S1 K100 + Q200 ASIC

Specialized Stacking hardware architecture

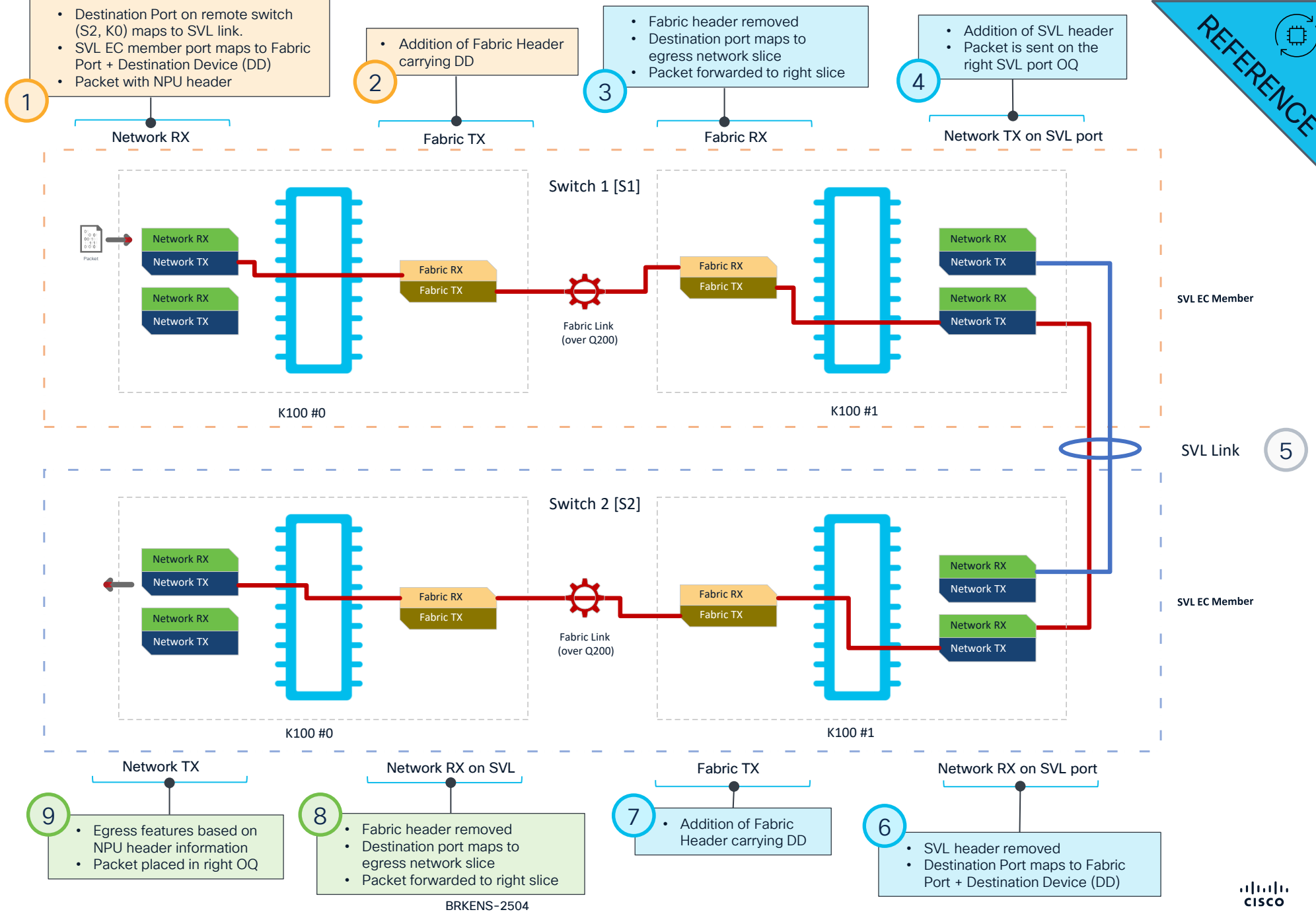
C9610-SUP-3 connects K100 ASIC 0, Slice 0 to System CPU

- Each K100 Network ASIC can process incoming Stack Headers.
- Packets destined for the local Switch ID will be forwarded internally between K100 ASICs (over the Q200 Fabric ASIC).
- Packets destined for the remote Switch ID will be encapsulated in VXLAN-GPE Stack header.
- SVL traffic uses a special QOS field and uses a dedicated QoS queue, to prioritize over regular traffic.



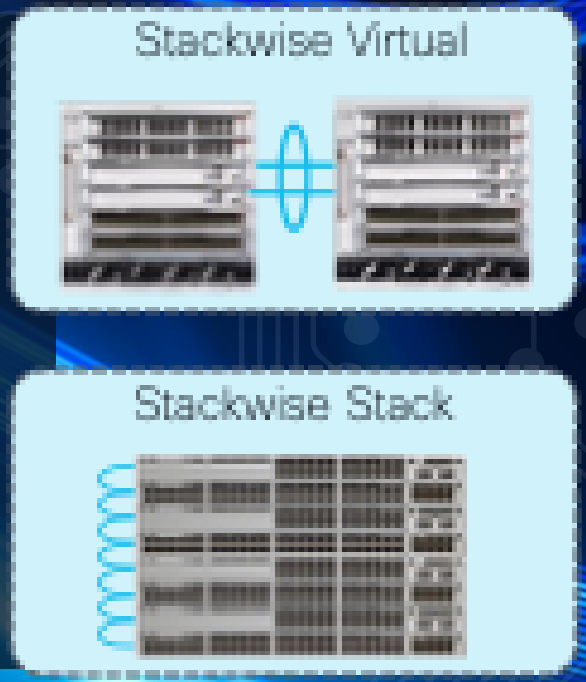
C9610 Stacking

Multi-ASIC Packet Walk



Cisco Smart Stacking

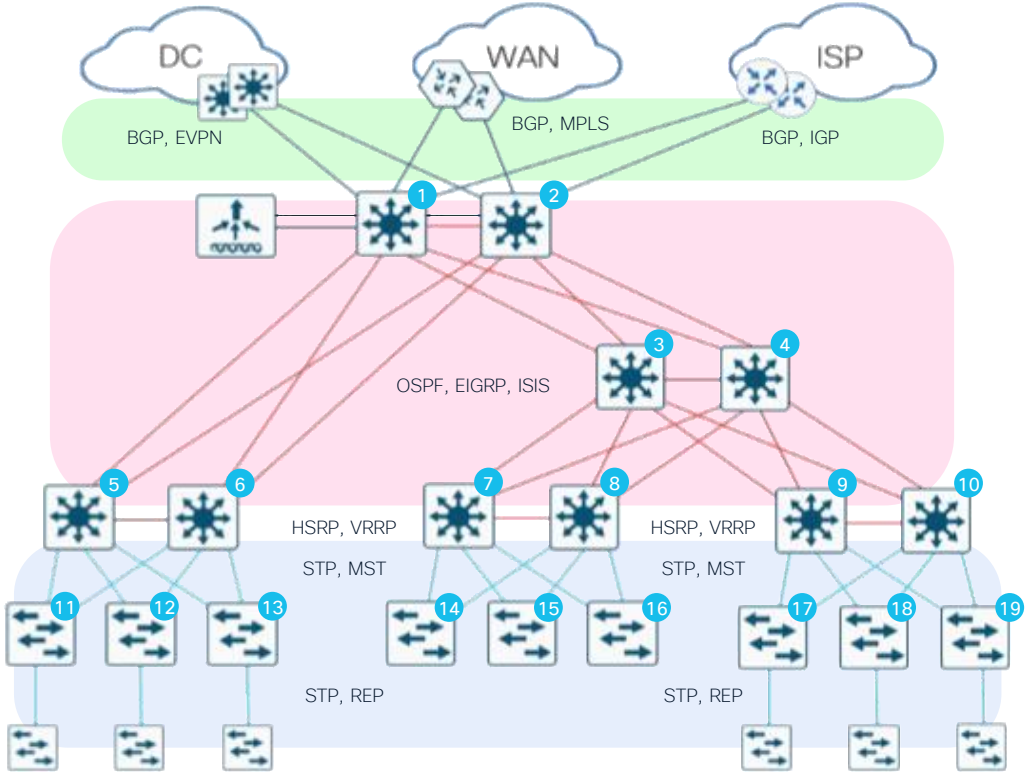
Campus Design with Smart Stacking



Campus Design with Smart Stacking

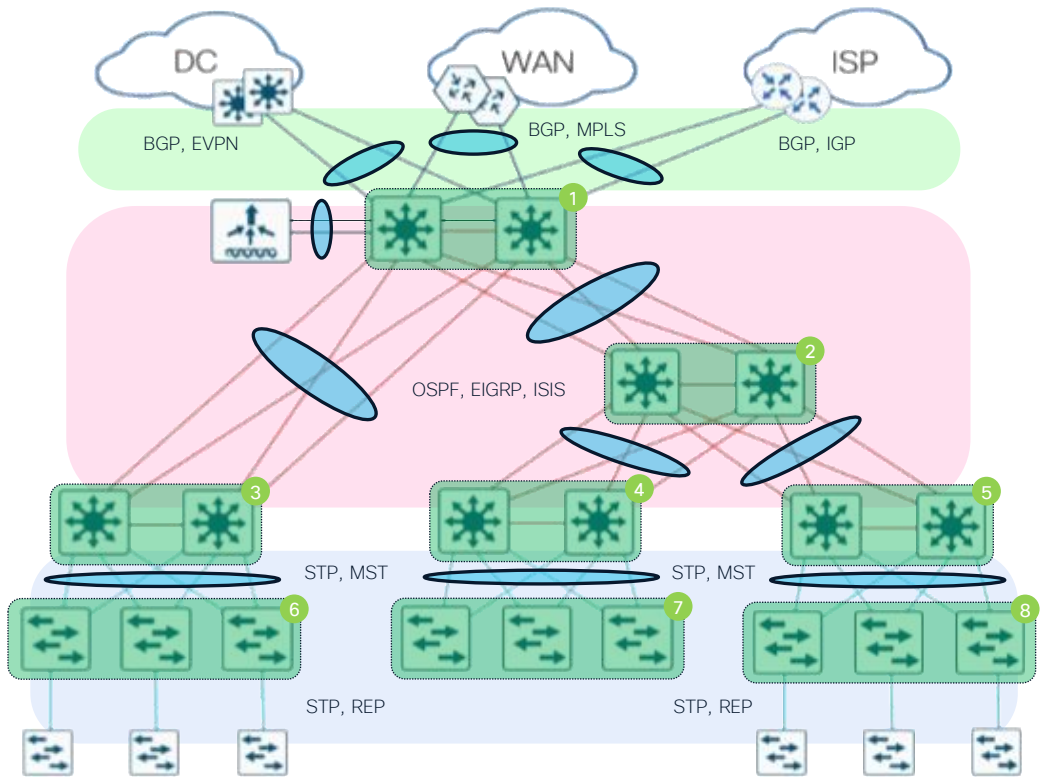
Reducing the number of Nodes & Peers, with superior L2 & L3 convergence

Traditional L2/L3 & ECMP



- ⚠ 19 Nodes to manage (IPs, Syslog, FNF, SNMP, YANG, etc.)
- ⚠ 7 Core IGP links & peers (10 IGP speakers)
- ⚠ 4 Distro STP links & peers (8 STP speakers)
- ⚠ Failover based on Protocol + ECMP (seconds)

Stacking L2/L3 & MEC

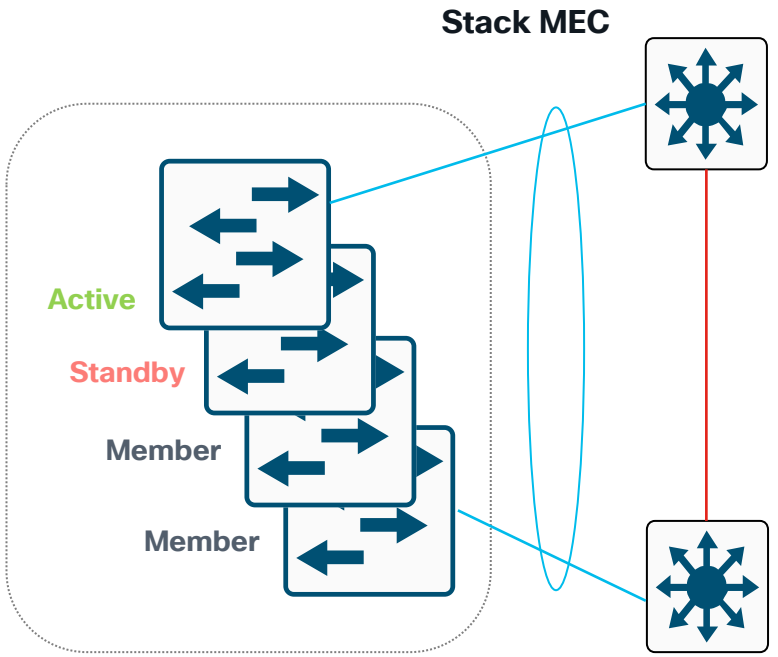


- ☑ 8 Nodes to manage (IPs, Syslog, FNF, SNMP, YANG, etc.)
- ☑ 3 Core IGP links & peers (4 IGP speakers)
- ☑ 1 Distro STP links & peers (5 STP speakers)
- ☑ Failover based on MEC (≤ 250 milliseconds)

Campus Access Resiliency

StackWise with Multichassis EtherChannel (MEC)

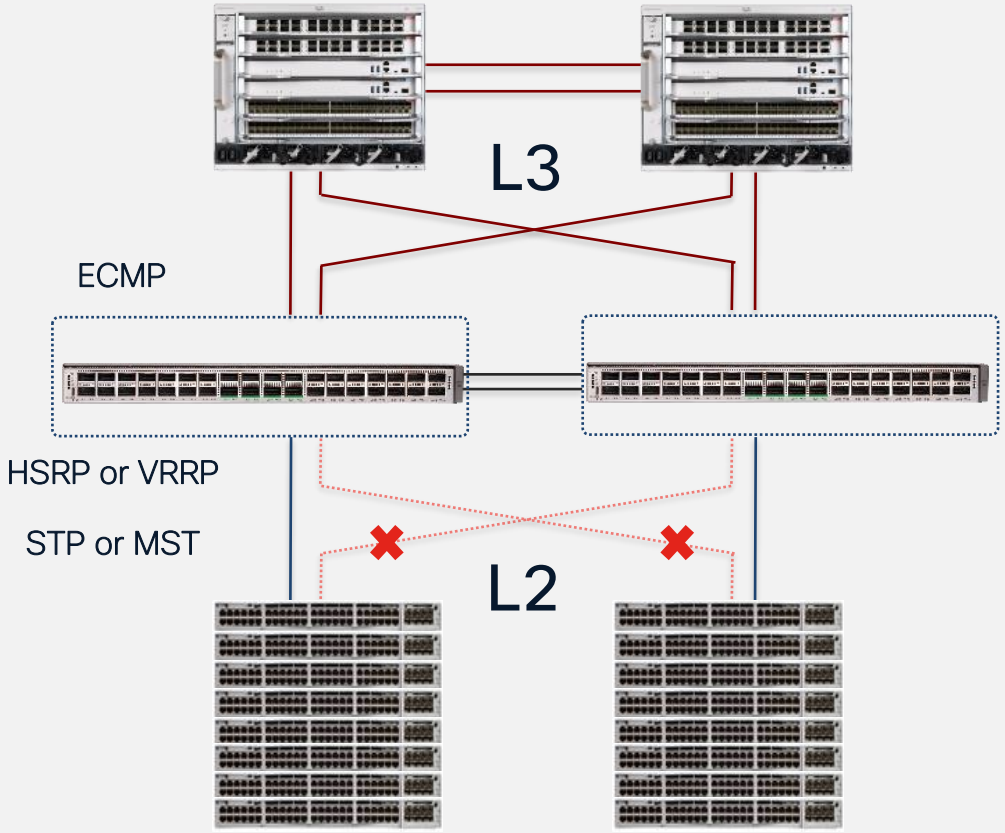
- Stacking allows up to 8 switches to be merged together physically, in a ring topology, to form a single, unified, virtual switch system.
- Provides a unified Control and Management plane by electing one switch as the SSO Active and another switch as the Hot-Standby.
  - Remaining switches become stack members
- Cross-switch Multichassis EtherChannel (MEC) extends EtherChannel link-aggregation by allowing member ports to be connected on different physical chassis.



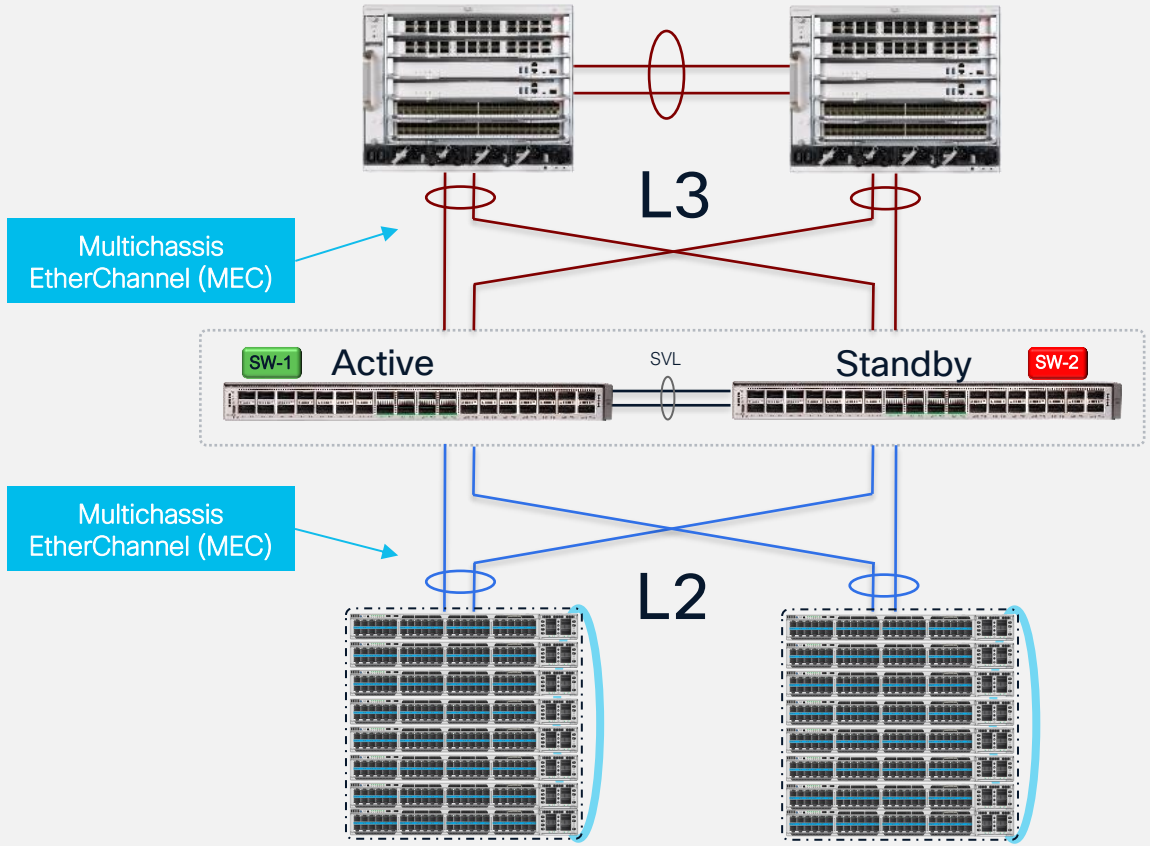
Single virtual switch Stack

Campus Core Resiliency

Traditional Design



Smart Stacking Design



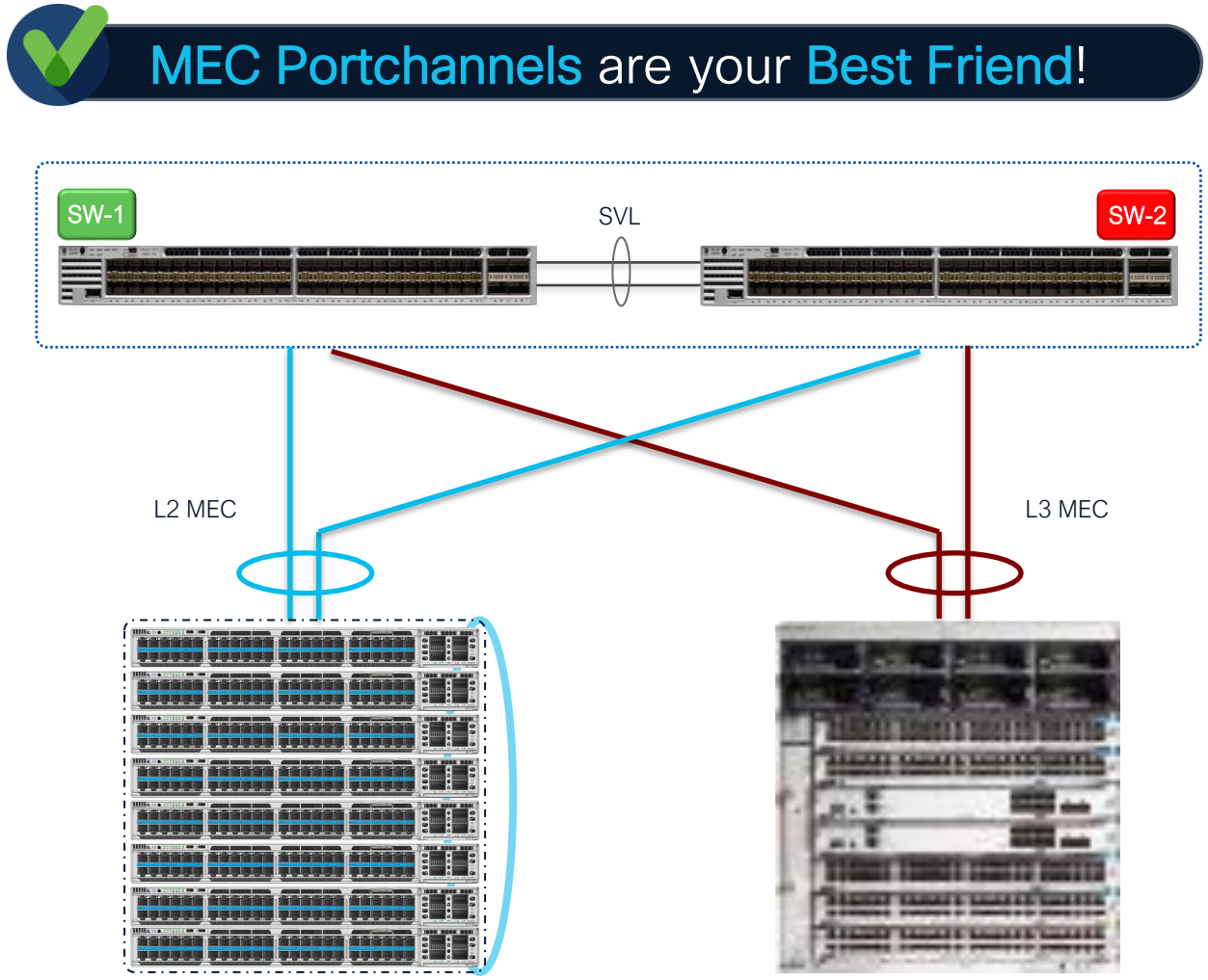
Simplify Operations by Eliminating STP, FHRP and Multiple Touch-Points

Double Bandwidth & Reduce Latency with Active-Active Multi-chassis EtherChannel (MEC)

Minimizes Convergence with Sub-second Stateful and Graceful Recovery (SSO/NSF)

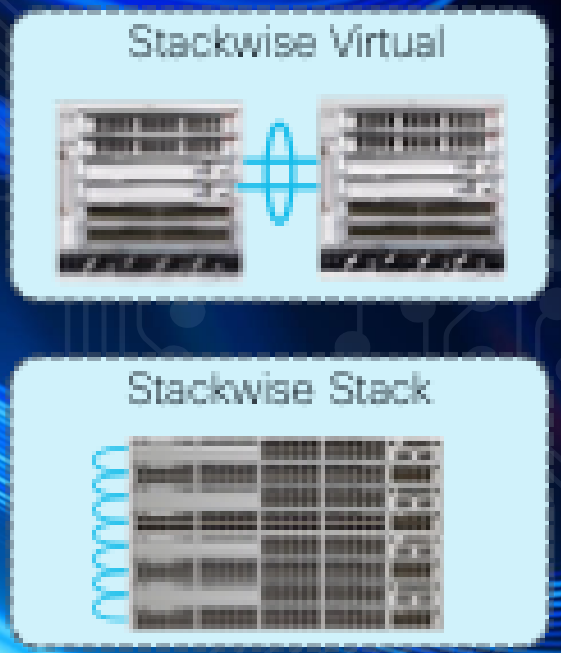
MEC Best Practices

- Multi-Chassis EtherChannel (MEC) enables cross stack-member link bundling into single logical L2/L3 Portchannel interface.
- Combining Stacking and Layer 2 or Layer 3 MEC builds simplified, scalable and highly resilient network.
- MEC is a primary network design aspect to enable:
  - Simplified STP loop-free network topology
  - Deterministic sub-second network recovery
  - Consistent L3 control-plane and network design as a traditional Standalone mode system
- StackWise Virtual supports 240 maximum MEC:
  - Port-Channel 1-240 available for L2/L3 network configurations
  - Port-Channel 241 is internally reserved for SVL purpose
- MECs can be deployed in three modes:
  - Cisco PAgP, LACP and Static (ON)



Cisco Smart Stacking

Summary & Reminders



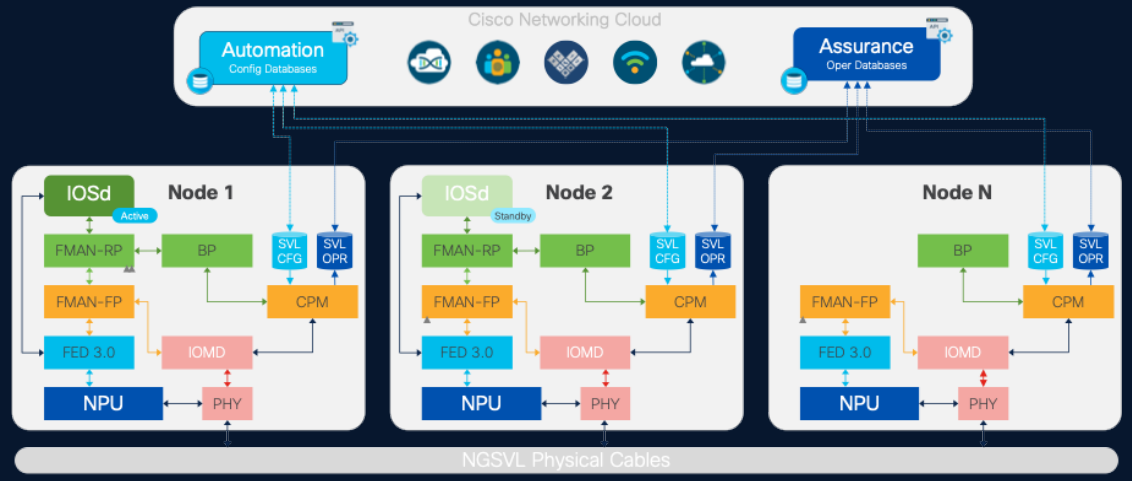
Introducing Smart Stacking (NG-SVL)

A new era of micro-services network device clustering

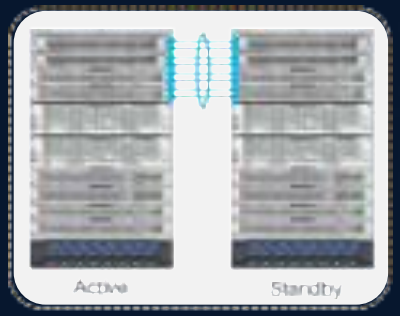
NEW

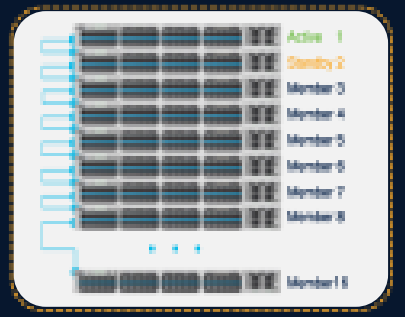
A new Stacking Architecture
based on standard ethernet protocols!

Cloud-Native IOSXE includes a new Stacking architecture based on standard **ethernet protocols** and **encapsulation**. Using either back-side or front-side ethernet ports for greater **scale**, enhanced **stability**, faster **SSO convergence**, and better **ISSU/XFSU** & **SMU** for hitless software upgrades.



C9610





C9350

How is the Architecture new?
- A new Bootstrap Process (BP) & Cluster Process Manager (CPM) - as a separate Linux thread
- Runs ISIS SPF + VXLAN-GPE on standard Ethernet

Is it front panel or back panel?
- Either! Dedicated cables or Transceivers + cables
- Stack Interface (SIF) is treated as an ethernet port

Can I still manage it the same?
- Familiar (same) config and show commands!
- Uses "*stackwise*" or "*stackwise-virtual*" CLIs

How does it benefit me?
- Common to both new C9350 & C9610
- Simplified cabling & dynamic link add/change
- Improved SSO and ISSU/SMU convergence

... and more, coming soon

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Thank You!


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