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https://ciscolive.ciscoevents.com/ciscolivebot/#BRKARC-2099

3
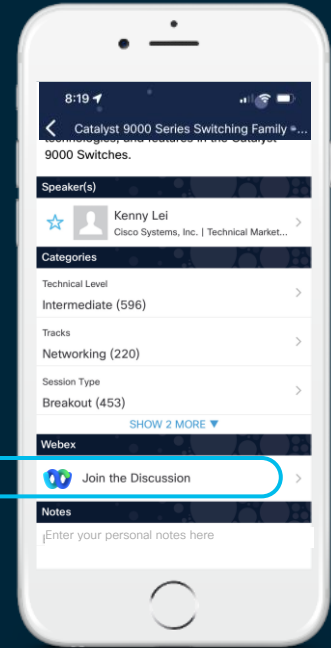
Agenda

- Digital trends

- Cisco ASICs

- Catalyst 9500X / 9500

- Catalyst 9600X / 9600

- Features and Scales

- Summary

    4

Digital trends shaping the future of business

Hybrid work
Work from home | Work from anywhere | Work from office

Industry 4.0
Wireless | Automation | Internet of Things | AI/ML

Hybrid cloud
Private cloud | Hybrid cloud | Public cloud

and the network is the core engine of hybrid work

New Access requirements for Future Campus

Distribution/Core/Edge
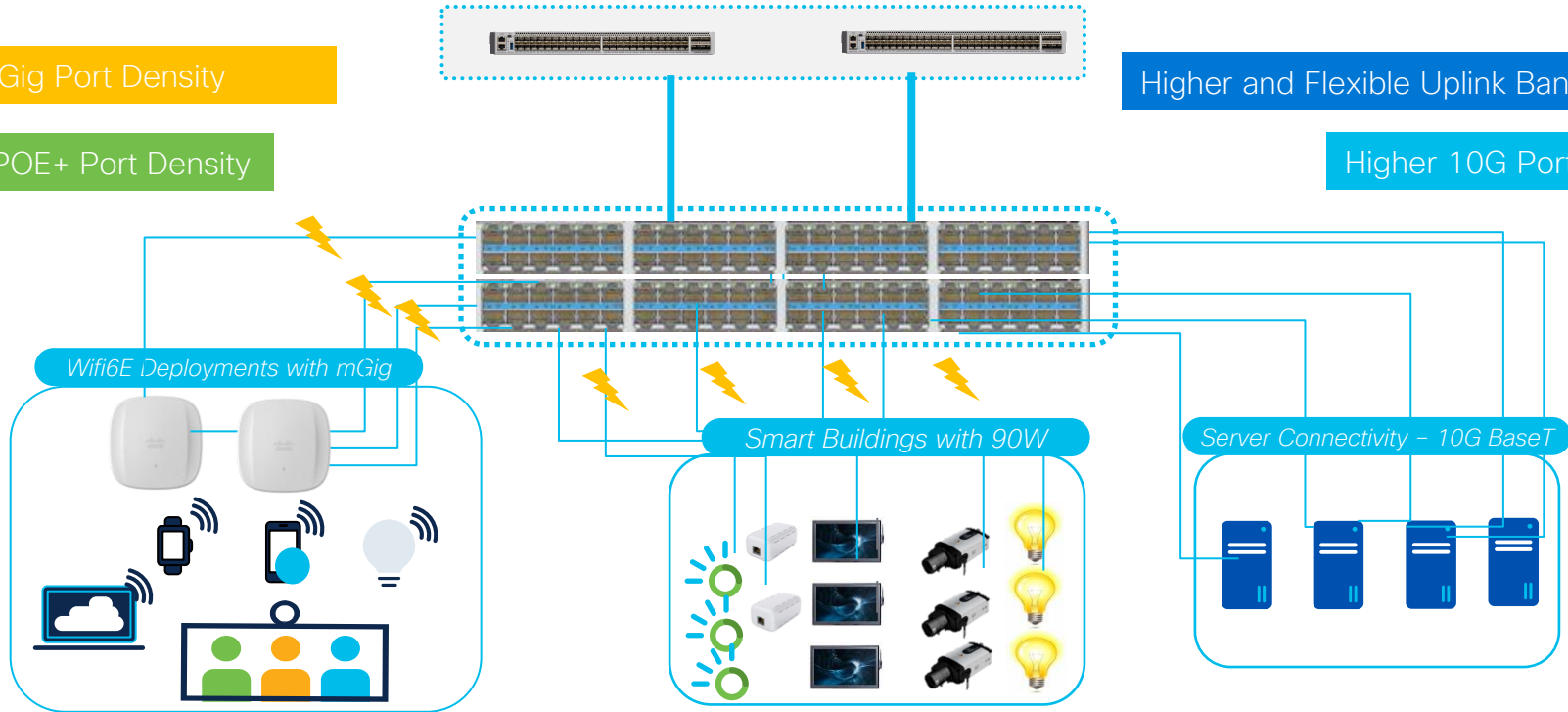
Higher Speeds, Scale, Buffer, etc.

Higher mGig Port Density

Higher and Flexible Uplink Bandwidth
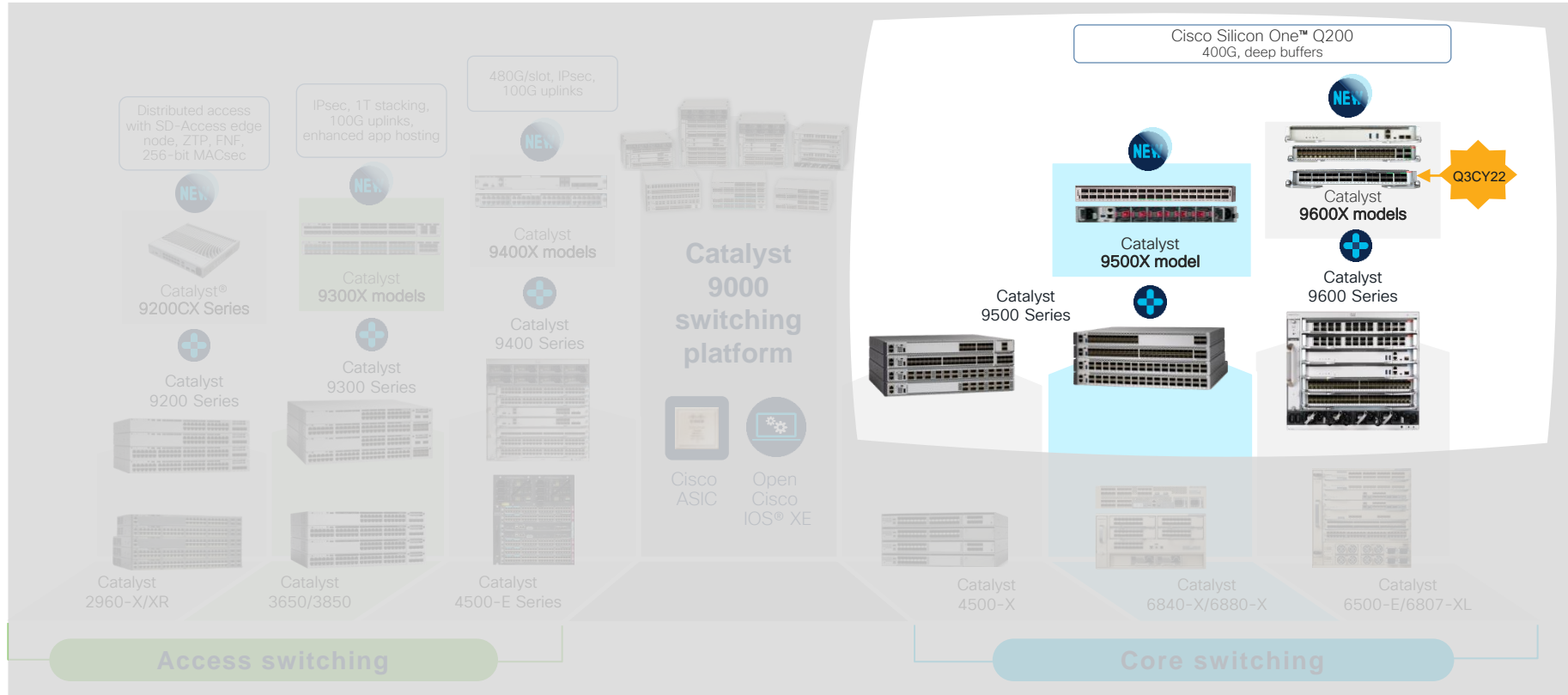
Higher UPOE+ Port Density

Higher 10G Port Density

Wifi6E Deployments with mGig

Smart Buildings with 90W

Server Connectivity – 10G BaseT

Catalyst 9000X – Expanding industry leadership

Adding the "X factor" to the industry's leading switching family

Cisco Silicon One™ Q200
400G, deep buffers

Distributed access with SD-Access edge node, ZTP, FNF, 256-bit MACsec

IPsec, 1T stacking, 100G uplinks, enhanced app hosting

480G/slot, IPsec, 100G uplinks

Catalyst® 9200CX Series

Catalyst 9300X models

Catalyst 9400X models

Catalyst 9000 switching platform

Catalyst 9500X model

NEW
Catalyst 9600X models

Q3CY22

Catalyst 9200 Series

Catalyst 9300 Series

Catalyst 9400 Series

Catalyst 9500 Series

Catalyst 9600 Series

Cisco ASIC

Open Cisco IOS® XE

Catalyst 2960-X/XR

Catalyst 3650/3850

Catalyst 4500-E Series

Catalyst 4500-X

Catalyst 6840-X/6880-X

Catalyst 6500-E/6807-XL

Access switching

Core switching

Cisco ASICs
Cisco UADPs and Silicon One

Catalyst 9000 Series – Common Building Blocks

Programmable x86 Multi-Core CPU

Application Hosting
Secure Containers

Open IOS XE® Polaris

Model-Driven APIs
Modular Patching

Cisco ASICs UADPs and Q200

Programmable Pipeline
Flexible Tables

Same binary image for both UADP and Silicon One C9K platforms*

* C9200 uses IOS XE Lite

UADP 3.0

~20B transistors
16-nm technology

Customizable ASIC templates

36-MB unified buffer

Double-width tables

3x more FIB scale

Up to 1.6 TB bandwidth

1G, 10G, 25G, 40G, and 100G speeds

Up to 1000Mpps throughput

Up to 1.6Tbps ASIC Interconnect

UADP 2.0XL and 3.0 ASIC comparison

Capabilities (per ASIC)	UADP 2.0XL	UADP 3.0
Switching and forwarding capacity	240 Gbps/360 Mpps	1.6 Tbps/1 Bpps
Stack bandwidth	2x 360 Gbps	2x 400 Gbps
Buffer capability	**2x 16 MB**	**36 MB shared buffer**
Switch Database Management (SDM) template	**Fixed templates**	**Customizable templates**
NetFlow capabilities	Dedicated NetFlow table	Shared NetFlow table
v4 FIB scale	Total 228,000*	Total 412,000*
v4 and v6 scale	**v6 reduced by half**	**v4 and v6 same scale**

* Maximum ASIC capability.

Cisco Silicon One™

Switching Silicon

- **High Throughput**
  extremely fast hardware-based L2-L4 forwarding and services (measured in Terabits per second)

- **Optimized Scale**
  optimized for Campus LAN environments with moderate IP & MAC scale (10s-100s of thousands)

- **Low Latency**
  extremely low hardware-based system latency (measured in Nanoseconds & Microseconds)

- **Streamlined Buffering**
  shallow buffering systems to reduce latency, with very high throughput

Silicon One™
Q200
©Cisco 2020

039

Routing Silicon

- **Flexible Features**
  complex, stateful L3-L7 forwarding and services (measured in Gigabits per second)

- **Massive Scale**
  optimized for WAN/SP environments with very high IP scale (100s of thousands - millions)

- **Mixed Interfaces**
  support for Ethernet, Serial, Cellular and other types and speeds in a single system

- **Deeper Buffering**
  deep buffers to accommodate different speeds, bursts and different flow patterns

Cisco Silicon One Bringing Switching and Routing convergence

Cisco Silicon One™ Q200
Industry leading Switching and Routing Silicon

12.8T BW

8.1 Bpps

8G HBM for deep buffers

2M IPv4 or 1M IPv6 route scale

Fully P4 Programmable Pipeline

50G PAM4 Serdes

Cisco Silicon ONE Q200

Industry Leading
12.8T System on Chip

First 7nm ASIC providing lowest watts/GE power consumption

Fully P4 programmable enabling feature velocity

Multi slice architecture for flexibility and scale

Routing Capabilities with Switching Power and Performance

Extending Cisco Catalyst 9500 & 9600 Series
Powered by Cisco Silicon One™ Q200 ASIC

C9500 & **C9600-SUP1**
(w/ UADP 3.0)

Optimized for Features

✓ **Speed**
- 1/10 & **25G** SFP
- 40 & **100G** QSFP

✓ **Scale**
- Upto **128K MACs**
- Upto **256K Routes**
- **108MB Buffers** (3x 36MB)

✓ **Services**
- L2/L3 Routing, MPLS
- LAN MACsec, Netflow, NAT
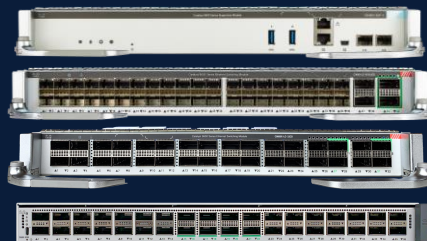- Custom ASIC Templates
- Campus Fabric (SDA & EVPN)

Double Existing Throughput

WAN MACsec, 1588v2 PTP

C9600X-SUP-2
C9600-LC-40YL4CD
C9600X-LC-32CD

10^x Routing & MPLS Scale

C9500X-28C8D

80MB Low-Latency + 8GB High-BW Buffers

50GE, 400GE, Coherent DWDM

C9500X & **C9600X-SUP2**
(w/ S1 Q200)

NEW

Optimized for Scale

✓ **Speed**
- 10/25G & **50G*** SFP
- 40/100G & **200***/400G QSFP

✓ **Scale**
- Upto **256K MACs**
- Upto **2M Routes**
- **80MB + 8GB Buffers**

✓ **Services**
- L2/L3 Routing, MPLS/TE
- LAN & **WAN-MACSec**, Netflow, NAT*
- Custom ASIC Templates
- Campus Fabric (SDA & EVPN*)

Maximum Investment Protection | 400G Leadership in Campus | Unmatched Flexibility

* Hardware capable

Cisco Catalyst 9500 Series
Purpose-built fixed core/aggregation switches

UADP 2.0XL	UADP 3.0	Silicon One Q200

UADP 2.0XL
- 40G at the price of 10G
- Industry's first 40G enterprise switch
- Optimized 10G switch for midsize backbone

C9500-16X
C9500-40X
C9500-24Q
C9500-12Q

UADP 3.0
- Up-to 48x 25 GE Ports
- Industry's first 100G enterprise switch
- Flexible templates

C9500-24Y4C
C9500-48Y4C
C9500-32QC
C9500-32C

Silicon One Q200
- Reversible Bi-directional Airflow
- Ultra Deep 8GB Buffers
- High route scale (2M) and Mac scale (256K)

C9500X-28C8D

Modular fans

Modular uplinks

Modular power supplies

Storage for application hosting

Catalyst® 9500X – Extending Cisco® Catalyst® 4500-X and 6800 Series leadership in fixed core
Up to 6 Tbps
Up to 8 Bpps
No oversubscription
8x 400GE Density
Pluggable SSD storage
USB 3.0
8x memory and 4x flash
8 core CPU
Customizable templates
Cisco StackWise® Virtual*

*Supported on 9500 and 9500H. Roadmap for 9500X

Catalyst 9500 Series
Extending the Catalyst 9500 High-Performance Fixed Core

Non-XL Scale

Catalyst 9500 High Perf.
(UADP 3.0)

C9500-32C / C9500-32QC

C9500-48Y4C / C9500-24Y4C

XL Scale

NEW

Catalyst 9500X
(S1 Q200)

C9500X-28C8D

Core + Edge

Total Capacity
3.2 Tbps
32 x 100G or
48 x 25G + 4 x 100G

2x

Total Capacity
6.0 Tbps
36 x 100G or
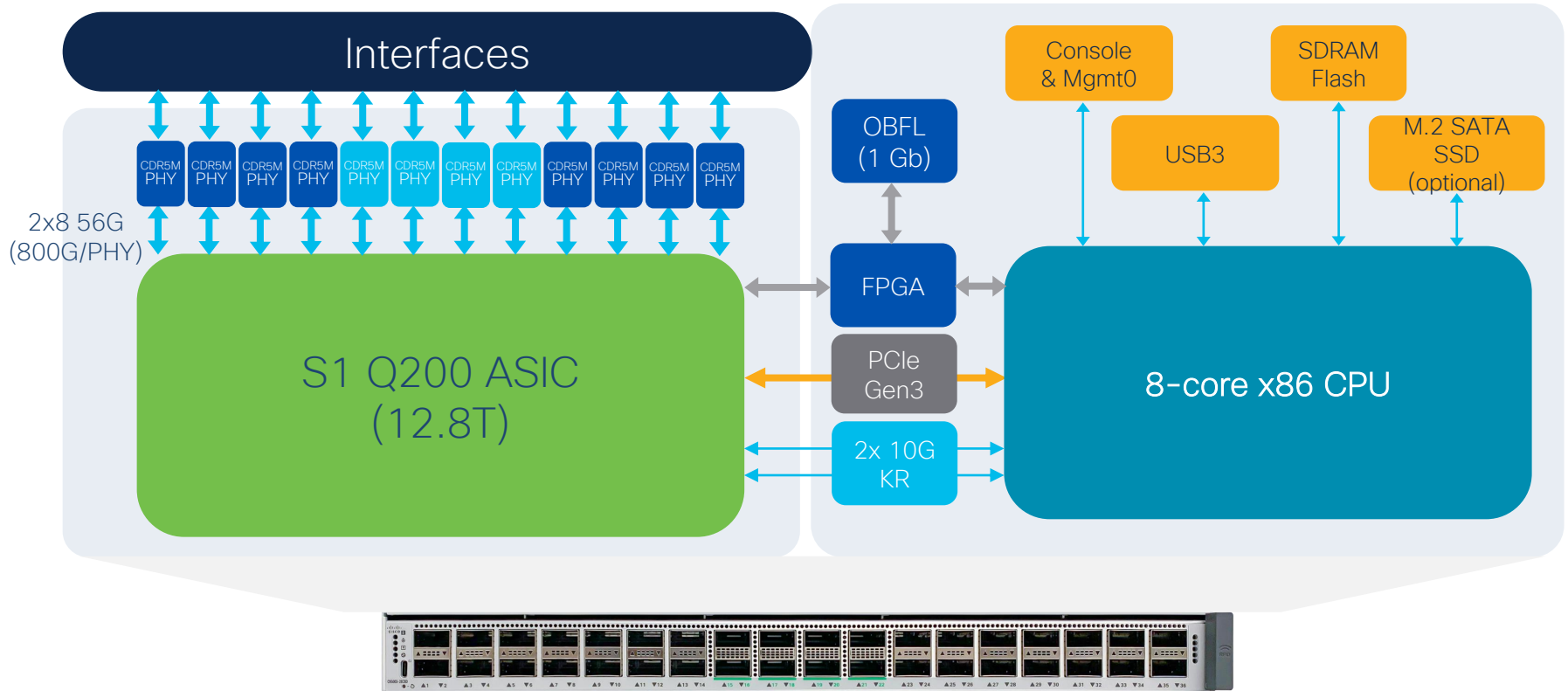28 x 100G + 8 x 400G

C9500X-28C8D
Gen2 Fixed 1RU QSFP Switch – 36x 100G / 28x 100G + 8x 400G

6.0 Tbps

- 1x **Cisco SiliconOne Q200** ASIC
  - **6.0 Tbps** System Throughput
  - **28x QSFP28** ports - 40/100GE
  - **8x QSFPDD** ports - 100/200*/400GE
- 1x **8C 2.4GHz x86** CPU with 2x **16GB (32GB) DDR4** DRAM
- **16GB Flash; Optional SSD (Up to 960G)**
- 12x **CDR5M** PHYs
  - MACSec, WAN-MACSec, ClearTag v3.4
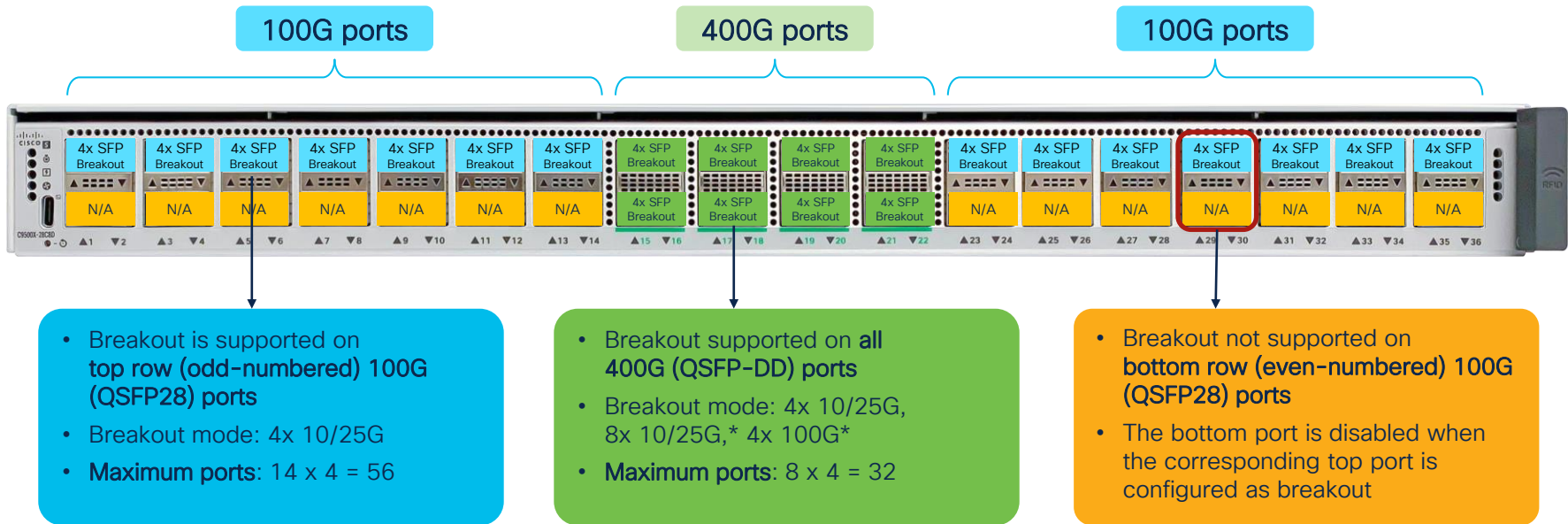 - IEEE 1588 & PTPv2*
- Various SFP Breakout & QSA support*
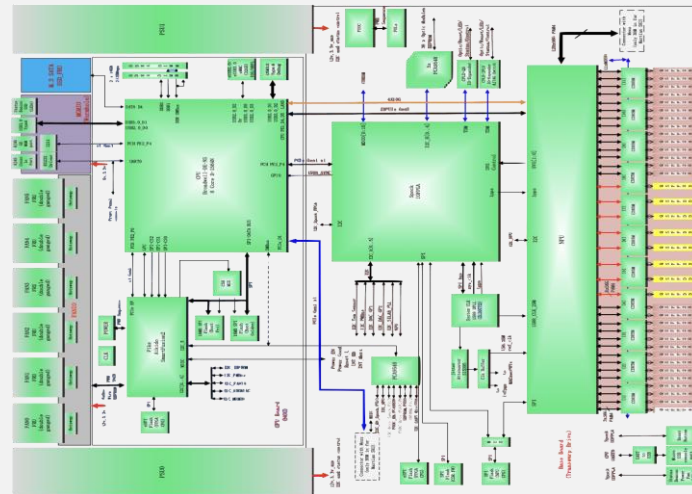
*Hardware capable

C9500X-28C8D Block Diagram

C9500X-28C8D
SFP breakout and QSA* support

100G ports   400G ports   100G ports

- Breakout is supported on **top row (odd-numbered) 100G (QSFP28) ports**
- Breakout mode: 4x 10/25G
- **Maximum ports**: 14 x 4 = 56

- Breakout supported on **all 400G (QSFP-DD) ports**
- Breakout mode: 4x 10/25G, 8x 10/25G,* 4x 100G*
- **Maximum ports**: 8 x 4 = 32

- Breakout not supported on **bottom row (even-numbered) 100G (QSFP28) ports**
- The bottom port is disabled when the corresponding top port is configured as breakout
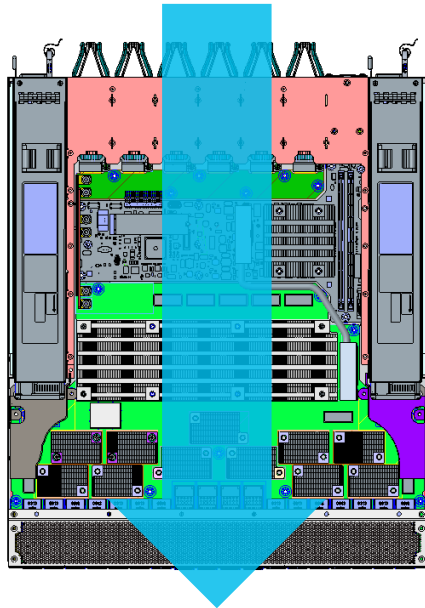
Maximum ports with breakout at FCS: 88 (56 +32)

* Hardware capable. System can support up to 120x 10/25G.

C9500X – Reversible Airflow

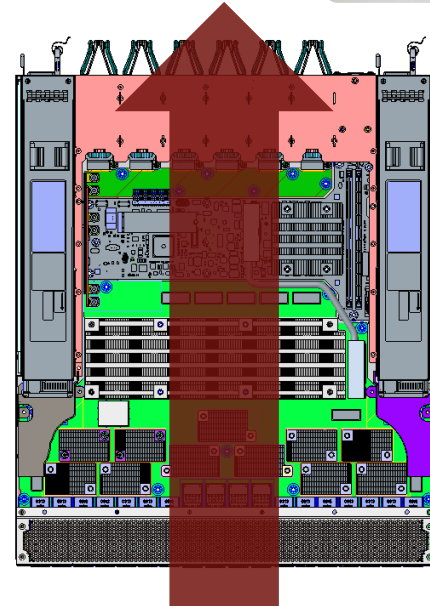**Back to Front**
Port-side Exhaust

Front to Back
Port-side Intake

NEW

- Color of Fan Unit handle/latch represents direction of airflow
- Different Fan PIDs for different airflow directions
  - Royal Blue – Back to Front
  - Burgundy – Front to Back
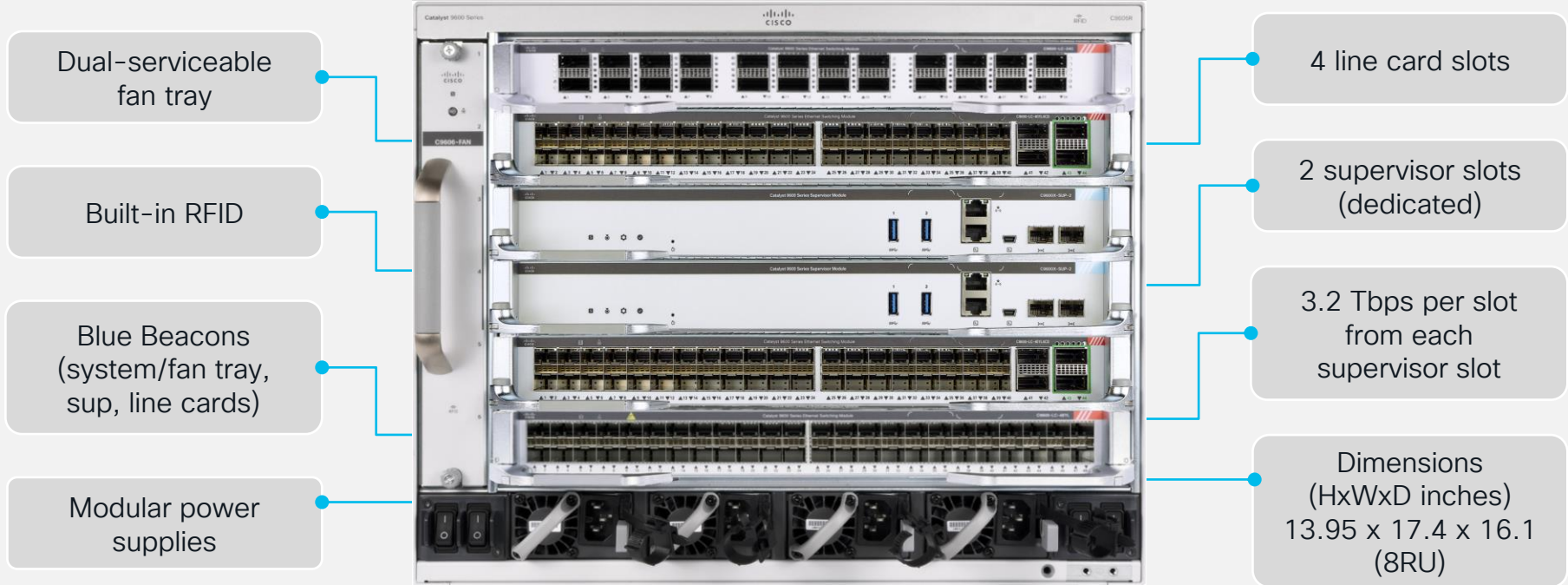- All Fans must be the same color (direction) to work correctly

Single **1500W AC/DC PSU** with Cisco Grey latch for both airflow directions

Catalyst 9600X/9600

Cisco Catalyst 9600 Series
Chassis

Dual-serviceable fan tray

Built-in RFID

Blue Beacons (system/fan tray, sup, line cards)

Modular power supplies

4 line card slots

2 supervisor slots (dedicated)

3.2 Tbps per slot from each supervisor slot

Dimensions (HxWxD inches) 13.95 x 17.4 x 16.1 (8RU)

Catalyst 9600 Series

Extending Modular Core with a Performance-Optimized Supervisor 2

UADP 3.0

SiliconOne Q200

Gen1
1.2T /slot

Gen2
3.2T /slot

NEW

Gen2
3.2T /slot

Gen1
1.2T /slot

Supervisor 1

Total Capacity

4.8 Tbps

Slot B/W

1.2 Tbps

Supervisor 2

Total Capacity

12.8 Tbps

Slot B/W

3x ## 3.2 Tbps

Cisco Catalyst 9600 Series
Supervisor 1
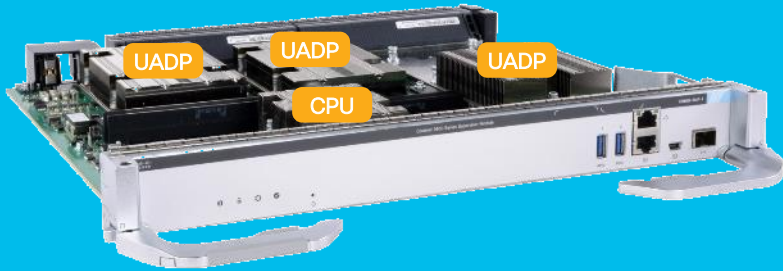
4.8 Tbps (full duplex)	1.2 Tbps per slot
3x UADP 3.0 ASIC	8 core X86 CPU @2.0 Ghz
M.2 SATA SSD (optional: up to 960G)	16G DDR4 memory
Built-in RFID	Mgmt ports: copper and fiber
Blue Beacon	2x USB3 1x mini-B USB console

Cisco Catalyst 9600 Series
Supervisor 2

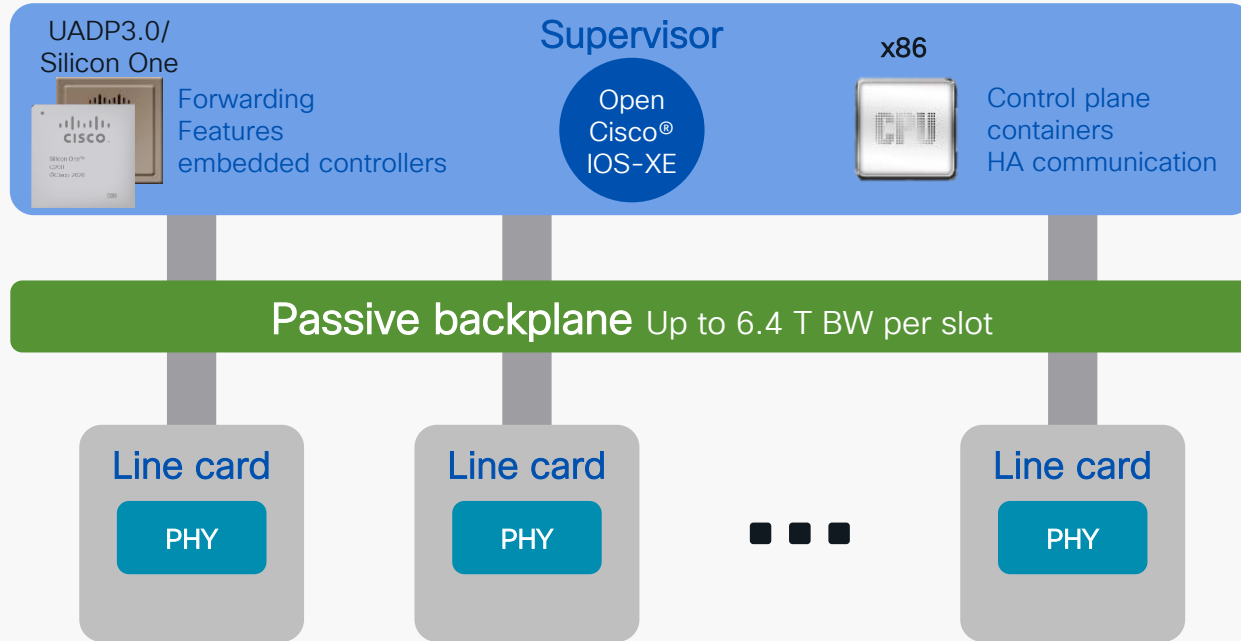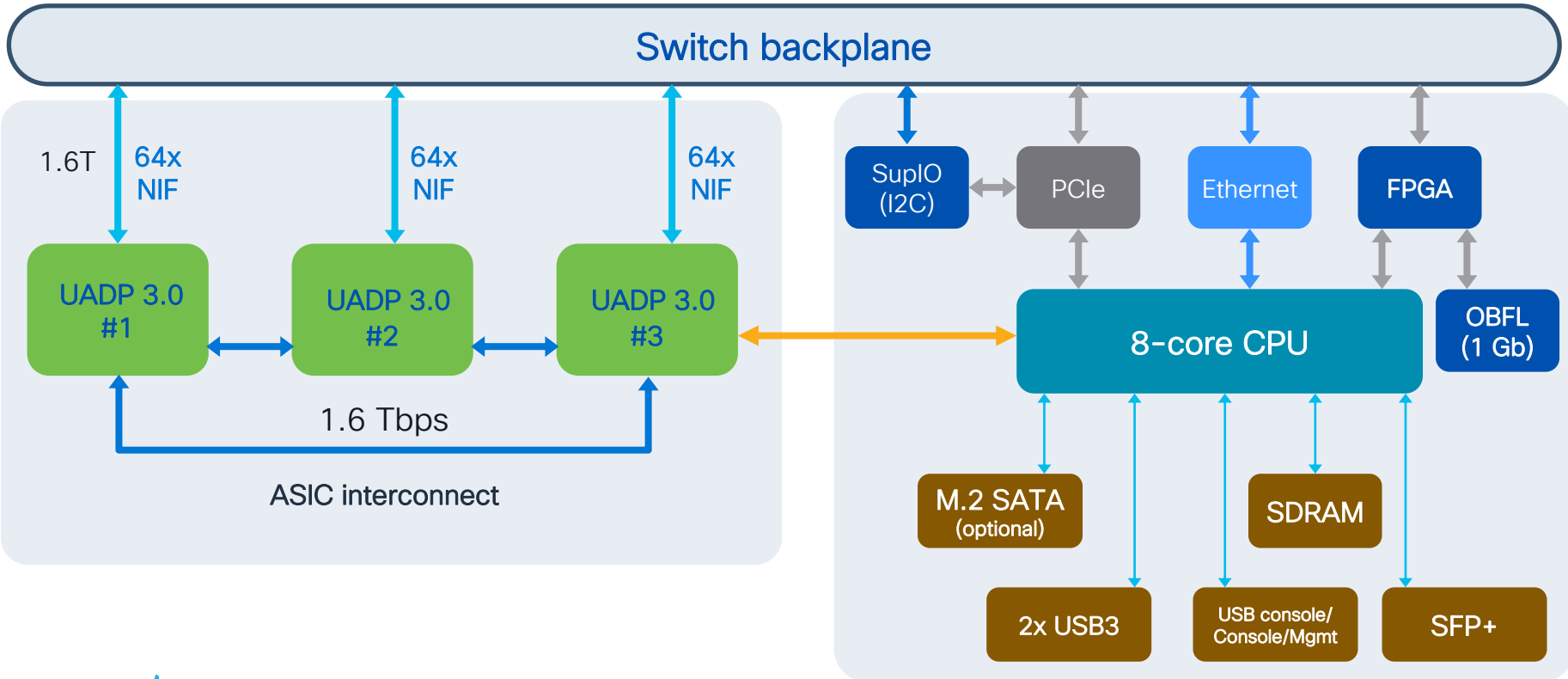|	
12.8 Tbps (full duplex)	3.2 Tbps per slot
1x Silicon One™ Q200 ASIC	8 core X86 CPU @2.7 Ghz
M.2 SATA SSD (optional: up to 960G)	32G DDR4 memory
Built-in RFID	Mgmt ports: copper and 2x10G fiber
Blue Beacon	2x USB3 1x mini-B USB console

Architecture

Centralized architecture

UADP3.0/
Silicon One

Forwarding
Features
embedded controllers

Supervisor

Open
Cisco®
IOS-XE

x86

Control plane
containers
HA communication

Passive backplane Up to 6.4 T BW per slot

Line card

PHY

Line card
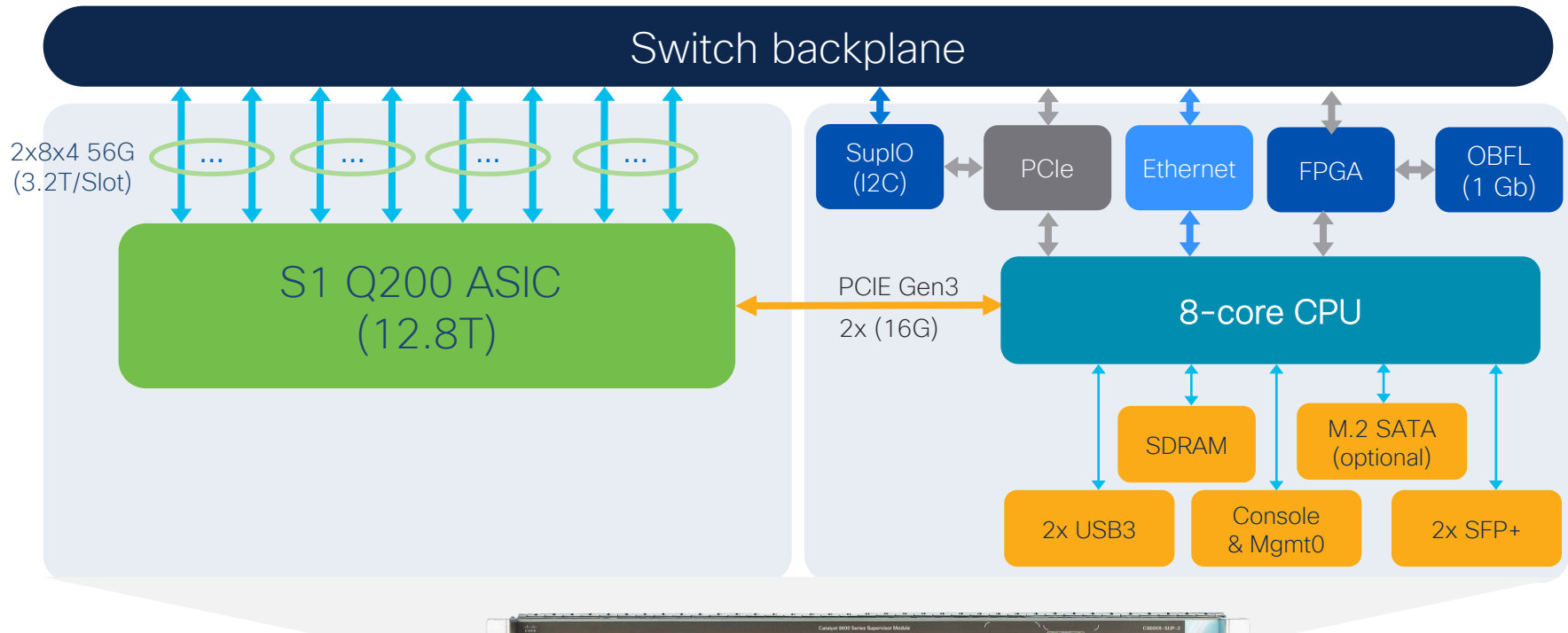
PHY

■ ■ ■

Line card

PHY

- Centralized architecture => **Uninterrupted supervisor switchover**

- Centralized architecture (Forwarding, queuing, and security are done on the supervisor) => **Unlock new capability** with a supervisor upgrade

- Transparent line cards => **Compatible** with new sup

- Passive backplane => **High MTBF**

- x86 CPU + storage => **App hosting**

Supervisor engine 1 – Block diagram

Switch backplane

1.6T 64x NIF 64x NIF 64x NIF

UADP 3.0 #1

UADP 3.0 #2

UADP 3.0 #3

1.6 Tbps

ASIC interconnect

SupIO (I2C)

PCIe

Ethernet

FPGA

8-core CPU

OBFL (1 Gb)

M.2 SATA (optional)

SDRAM

2x USB3

USB console/ Console/Mgmt

SFP+

C9600X-SUP-2 Block Diagram

Switch backplane

2x8x4 56G
(3.2T/Slot)

... ...

S1 Q200 ASIC
(12.8T)

SupIO
(I2C)

PCIe

Ethernet

FPGA

OBFL
(1 Gb)

PCIE Gen3
2x (16G)

8-core CPU

SDRAM

M.2 SATA
(optional)

2x USB3

Console
& Mgmt0

2x SFP+

Catalyst 9600/X:
Introducing the first 400G line cards in campus

Shipping

Catalyst® 9606R

C9600-LC-24C

C9600-LC-48YL

C9600-LC-48S

C9600-LC-48TX
(Multigigabit)

Combo line cards

C9600-LC-40YL4CD

NEW

3.2 Tbps with SUP-2
1.2 Tbps with SUP-1

C9600X-LC-32CD

Q3CY22

With SUP-2 only (3.2Tbps)

Provides for **uplink requirement** without using additional slot

Dual-personality line card

Flexible speed support

Lower total BoM cost, save on additional line cards

C9600-LC-40YL4CD
Gen2 Combo Line-Card – 40xSFP56 + 2xQSFP56 + 2xQSFPDD

3.2 Tbps

- **3.2 Tbps** With Gen2 Sup
  - 40x **SFP56** ports - 10/25/50*GE
  - 2x **QSFP56** ports - 40/100/200*GE
  - 2x **QSFPDD** ports - 40/100/200*/400GE
- **1.2 Tbps** With Gen1 Sup
  - 40x **SFP28** ports - 1/10/25GE
  - 2x **QSFP28** ports - 40/100GE
- 8x **CDR5M** PHYs
  - MACSec, WAN-MACSec, ClearTag v3.4
  - IEEE 1588 & PTPv2*
  - Hitless MUX (HMUX)
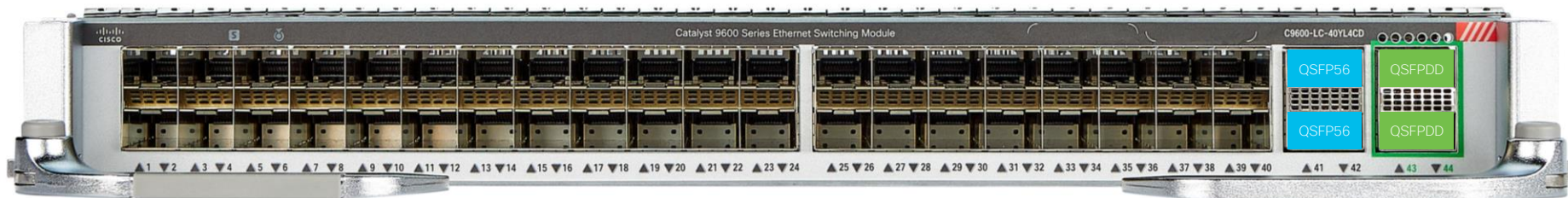- Various Breakout & QSA support (QSFP ports)*
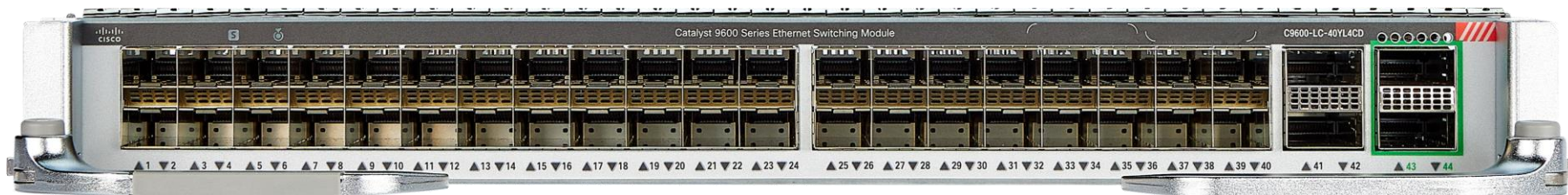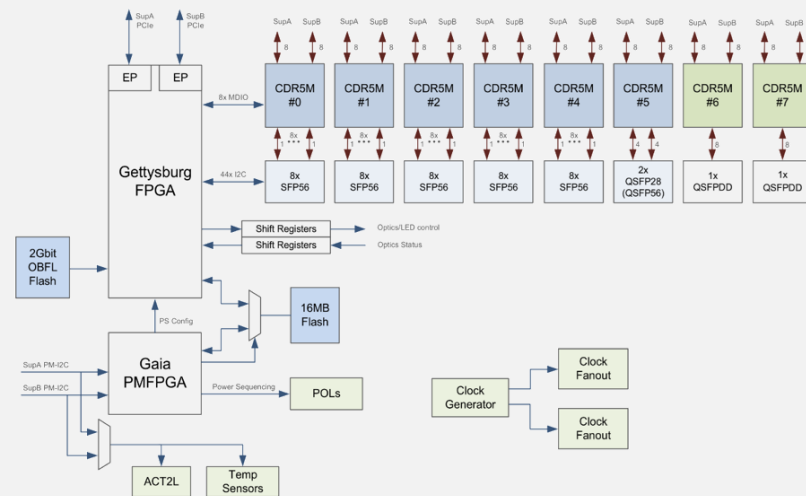
* Hardware capable

C9600-LC-40YL4CD Ports and Speeds Support

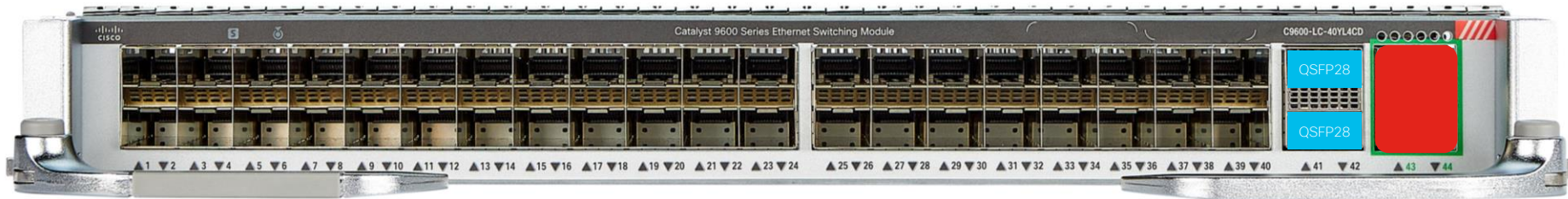with **Sup2**: 3.2Tbps

40x 10/25/50*GE + **2**x 40/100/200*GE + **2**x 40/100/200*/400GE

IOS-XE 17.7.1

with **Sup1**: 1.2Tbps

40x 1/10/25GE + **2**x 40/100GE

IOS-XE 17.8.1

* Hardware capable

C9600X-LC-32CD
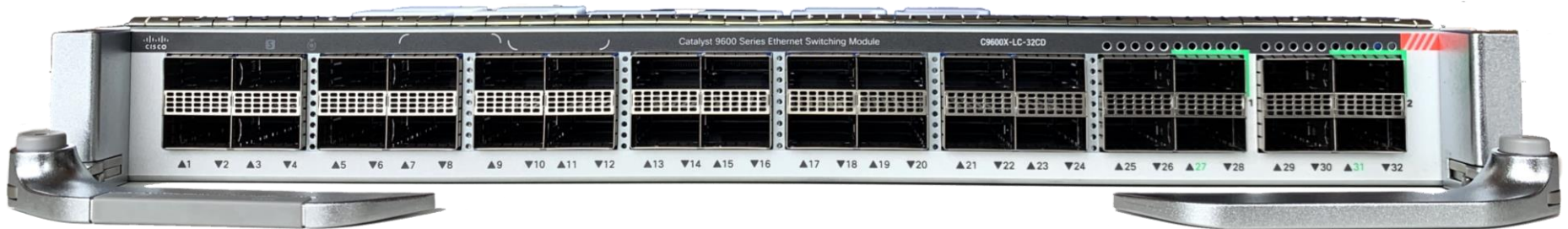## Gen2 Module – 30 x QSFP28 + 2 x QSFP-DD

3.2 Tbps

- **3.2Tbps with Supervisor 2 Only**
  - 30 x QSFP28 ports, 40/100GE
  - 2 x QSFP-DD ports, 40/100/200*/400GE
- **NOT supported with Supervisor 1**
- **8 x CDR5M + 2 x CDR5L PHYs**
  - MACSec, WAN-MACSec, ClearTag v3.4
  - IEEE 1588 & PTPv2 (Precision Time Protocol)
  - Hitless MUX (HMUX)
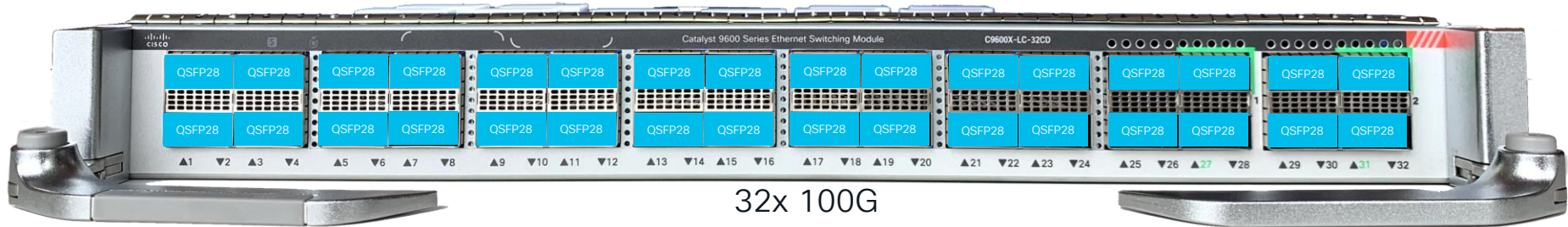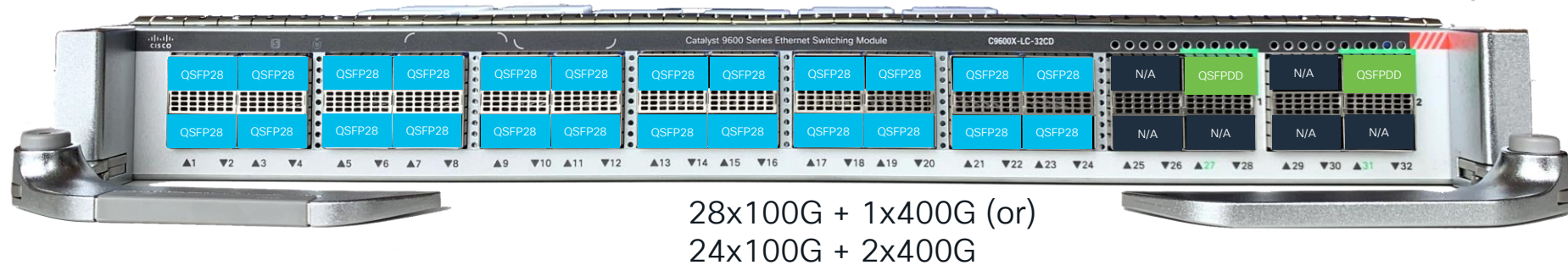
✔ Supervisor 2

✘ Supervisor 1

* Hardware capable

C9600X-LC-32CD
100G / 400G Port Modes
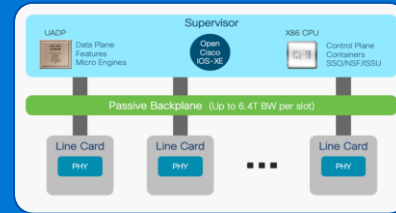
All 100G (QSFP28) Mode (Default):

32x 100G

Two 400G (QSFP-DD) Mode:

28x100G + 1x400G (or)
24x100G + 2x400G

Gen1 Line-Cards Support with SUP2

Centralized Architecture
- **Gen1 Line-Cards supported***
- Only PHYs on the Line-Cards
- All forwarding on the Supervisor (ASIC)

Additional Bandwidth ☺
- C9606 backplane traces support up to 56G PAM4
- Gen1 Line Cards now support up to 2.4T per Slot
  - **24 x 100G** QSFP on LC-24C
  - **48 x 50G**** SFP on LC-48YL
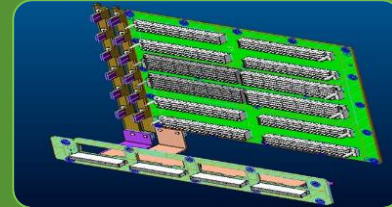
No MACsec support ☹
- Q200 does not have onboard Crypto engine
  - Gen2 LCs use newer CDR5M PHY for MACsec
- UADP has onboard MACsec engine
  - Gen1 LCs use older CDR4 PHY (not MACsec capable)
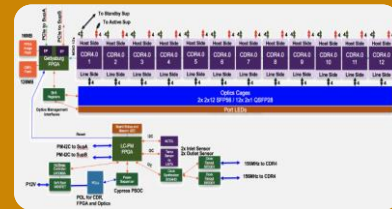
* C9600-LC-48S is not supported with Sup2

** Hardware capable

Catalyst 9600 Line Card Support Matrix

	C9606 Chassis	
	C9600-SUP- 1	**C9600X-SUP- 2**
C9600-LC-24C	✔️ 24x 40G or 12x 100G	✔️ 24x 40G/**100G** (No MACsec)
C9600-LC-48YL	✔️ 48x 1/10G and 25G	✔️ 48x 10/25G and **50G*** (No MACsec, no 1G)
C9600-LC-48TX	✔️ 48x 1/2.5/5G and 10G (Multigigabit)	✔️ 48x 10G (No MACsec, no 1/2.5/5G)
C9600-LC-48S	✔️ **48**x **1G SFP**	❌
C9600-LC-40YL4CD	✔️ 40x 1/10G and 25G + 2x 40G and 100G	✔️ 40x 10/25G and **50G*** + 2x 40/100G and **200G*** + 2x 40/100/**200G*** and **400G** MACsec and **WAN MACsec** (no 1G)
C9600-LC-32CD	❌	✔️ 30x 40/100G + 2x 40/100/**200G*** and **400G** MACsec and **WAN MACsec** (no 1G)

TIP

SUP2 hardware does not support 1GE or below speeds natively

If 1GE downlinks are required, use SUP1

NEW

Q3CY22

* Hardware capable

Features and Scales

Features and Scales

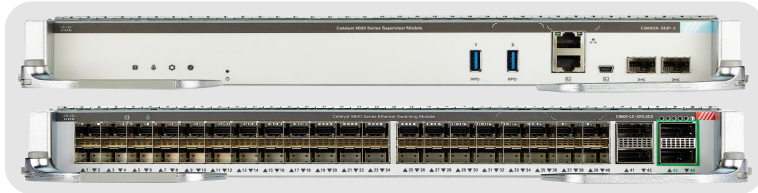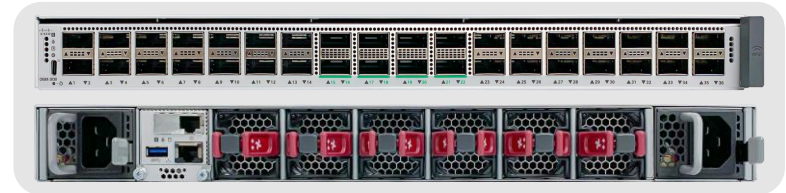|	Silicon One Q200		UADP 3.0	
	Default	**Maximum** (Custom)	**Default**	**Maximum** (Custom)
MAC Addresses	128K	256K	80K	128K
IP Host Routes	128K	256K	80K	128K
Multicast L2 groups	16K	64K*	16K	48K
Multicast L3 routes	32K	64K*	32K	48K
IP LPM Routes	2M	2M	212K	256K
MPLS Labels	256K	512K	32K	64K
SGT/OG Labels	32K	64K	32K	64K
NAT* Sessions	16K*	128K*	3K	16K
Sec ACL Entries	8K	10K*	12K	27K
QoS ACL Entries	8K	10K*	8K	21K
PBR* ACL Entries	8K*	10K*	3K	16K

* Hardware capable on Q200

Catalyst 9500X & 9600X – Things to know
Next Generation Core + Edge Switching with Silicon One™ Q200
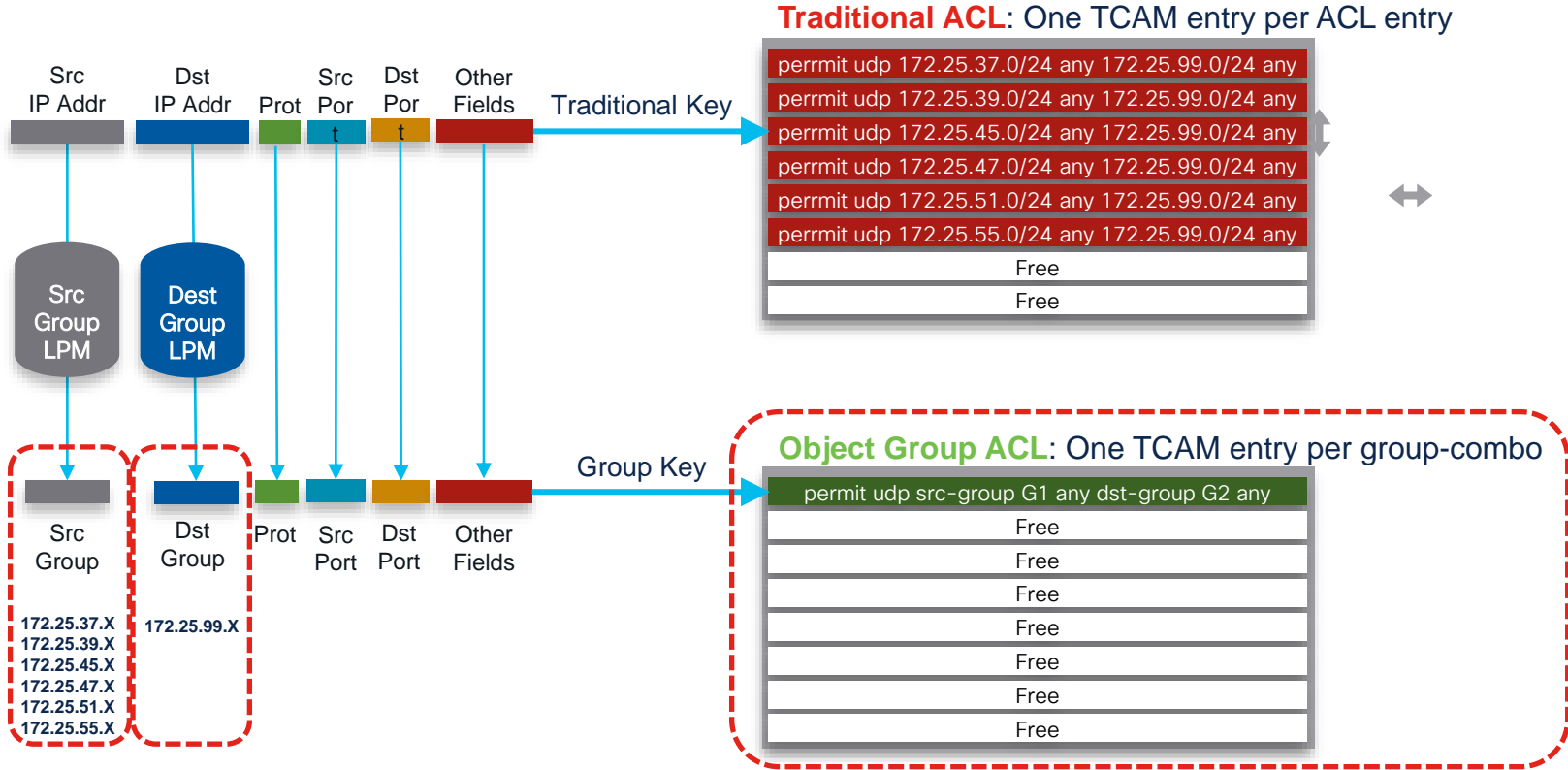
TIP

C9600X-SUP-2 + LC-40YL4CD

C9500X-28C8D

Technology	Brief Description	Diffs from UADP 3.0
✔ Large LPM Table	• Up to 2M IPv4 or 1M IPv6 (hash efficiency is about 80%) • Dedicated Memory for LPM	• Up to 256K IPv4/IPv6 with Custom SDM template • LPM and other features share 416K ASIC memory
✔ Large MAC Table	• Up to 256K MAC entries Custom SDM template. • Shared with other features	• Up to 128K MAC entries with Custom SDM template • MAC shared with LPM, etc. in same 416K ASIC memory
✔ VoQ QoS + HBM	• Q200 has 80MB local (low-latency) + 8GB HBM (High Bandwidth Memory) buffer memory. • Q200 uses a Virtual Output Queue (VoQ) architecture. All queuing and policing policies applied on Ingress.	• Max 36MB unified buffer memory per ASIC • Supports both Ingress/Egress queuing & policing
✔ OGACL & SGACL	• 8K IPv4, 4K IPv6 ACL TCAM entries. • Object-Group & Security-Group ACLs use CEM to map IP-to-Group label, TCAM only uses L4 ACEs. (OG/SG ACL design is optimal for layer 3 environment).	• 64K ACL TCAM entries per ASIC • Object-group expand into the TCAM space
✔ LAN & WAN-MACsec	• Q200 does not have built-in crypto engine. • C9500X & C9600X-LC uses new CDR5M PHY (400Gbps Full-Duplex). CDR5M provides line-rate (8x 400G = 3.2T) 802.1ae (LAN) MACsec and WAN-MACsec.	• UADP3 has built-in MACsec crypto (speed of ASIC) • UADP3 only supports LAN MACsec (no WAN-MACsec)
✔ Flexible NetFlow*	• Q200 does not have built-in Flow Cache memory (no hardware-based Netflow). • C9500X & C9600X uses new Software-based FNF (≤ 2M entries), with a dedicated CPU core (~2Mpps). FNF sampler rate 1:1000, ~10Tbps of 512-Byte packets = ~2Mpps.	• UADP3 has built-in (HW) FNF, max 64K entries per ASIC • FNF shared with LPM, etc. in same 416K ASIC memory

* Roadmap

CISCO *Live!*

Why OGACL/SGACL in Campus Core?

Object-Group ACLs for IP

C9500X/9600X
Core Switches

WAN/DC/SP

IP
Network

Clients = OGID

C9300X/9400X
Access Switches

Scalable-Groups for SDA

C9500X/9600X
CP/Border Nodes

C   B   C   B

DNA Center

E   E   E

SDA
Fabric

WAN/DC/SP

Policies (120)

Clients = SGT

C9300X/9400X
Edge Nodes

Object-Groups map IP/mask to Labels in CEM

- User defines IP/masks to simple OG name
- OGID labels are stored in Exact Match table

OGACL ACEs take minimal space in ACL TCAM

- Only the Permit/Deny ACEs in TCAM
- OGACLs with same ACEs can reuse entries

Scalable-Groups map IP/mask to Labels in CEM

- ISE/DNAC defines IP/masks to simple SG name
- SGT labels are stored in Exact Match table

SGACL ACEs take minimal space in ACL TCAM

- Only the Permit/Deny ACEs in TCAM
- SGACLs with same ACEs can reuse entries

Traditional ACL vs Group-Based ACL

Src IP Addr	Dst IP Addr	Prot	Src Port	Dst Port	Other Fields

Traditional Key →

Traditional ACL: One TCAM entry per ACL entry

perrmit udp 172.25.37.0/24 any 172.25.99.0/24 any
perrmit udp 172.25.39.0/24 any 172.25.99.0/24 any
perrmit udp 172.25.45.0/24 any 172.25.99.0/24 any
perrmit udp 172.25.47.0/24 any 172.25.99.0/24 any
perrmit udp 172.25.51.0/24 any 172.25.99.0/24 any
perrmit udp 172.25.55.0/24 any 172.25.99.0/24 any
Free
Free

Src Group LPM

Dest Group LPM

Src Group	Dst Group	Prot	Src Port	Dst Port	Other Fields

172.25.37.X
172.25.39.X
172.25.45.X
172.25.47.X
172.25.51.X
172.25.55.X

172.25.99.X

Group Key →

Object Group ACL: One TCAM entry per group-combo

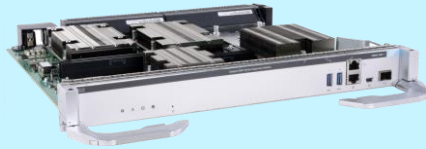| permit udp src-group G1 any dst-group G2 any |
|---|
| Free |
| Free |
| Free |
| Free |
| Free |
| Free |
| Free |

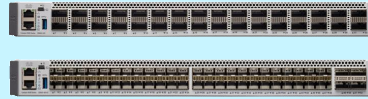# Catalyst 9500/X & 9600/X Series Core Positioning

Next Generation Core + Edge Switching with Silicon One™ Q200

Feature Optimized
C9500 & C9600-SUP-1

C9600-SUP-1   C9500

- ✓ Best-in-class Enterprise Core feature set
- ✓ Low speeds (1G – 40G) and port density
- ✓ Comprehensive MPLS, EVPN and SDA
- ✓ Ideal for Campus Core, Collapsed Core + Agg

Ideal for C6K non-XL deployment migration

Performance Optimized
C9500X & C9600X-SUP-2

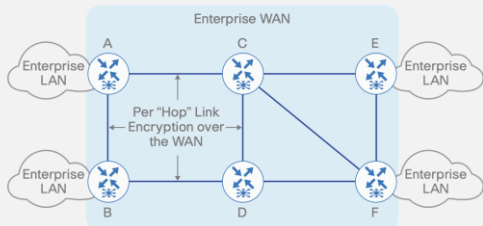### C9600X-SUP-2   C9500X

- ✓ Unmatched forwarding scale and performance
- ✓ High speeds (10G – 400G) and port density
- ✓ Scaled MPLS and SDA, WAN-MACsec
- ✓ Ideal for Campus Core + Edge, or Centralized WLC

Ideal for C6K XL deployment migration

WAN MACsec overview and use cases
Enabled in hardware on Catalyst 9000 Switches

MACsec

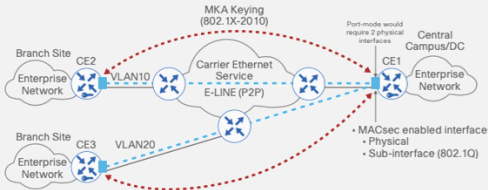Enterprise WAN

Per "Hop" Link Encryption over the WAN

- Hop-by-hop encryption
- Directly connected Layer 2 links **only**
- Secure any direct link in campus/ WAN, including DWDM
- 256/128-bit AES encryption

Supported on **all Catalyst® 9000** models
All ports and speeds simultaneously

WAN MACsec

MKA Keying (802.1X-2010)

- End-to-end encryption across Layer 2 Ethernet WAN service
  - EoMPLS/VPLS, Q-in-Q
  - Point-to-point or point-to-multipoint
- Applications include secure site interconnect, DCI, storage replication
- 256/128-bit AES encryption

Catalyst 9600X   Catalyst 9500X

Supported on **Silicon One™** platforms*
All ports/speeds (up to 400G) simultaneously

* Requires Release 17.8.1 and HSEC key ($1 PID).

App Hosting on C9K Switches

Existing Hardware

Managed via CLI
or Cisco DNA Center

Real Time Processing

Lower Latency

Save Bandwidth

IT Operations and
Monitoring Tools

Consolidate Physical Infrastructure

ThousandEyes
kibana
WIRESHARK
perfSONAR powered

Security Agents
and Functions

Enhance Visibility & Security Enforcement

Attivo NETWORKS
TRAPX SECURITY

Cloud Gateways with
Serverless Edge Compute

Reduce App Latency & Optimize App Traffic

Cybervision
Cisco DNA Spaces
NS1.
Alleantia ALL <THINGS> JOINED

Customer Specific
Applications

3rd Party App Hosting

Rich ecosystem partnership with 25+ certified apps and 200+ active customer

App Hosting

	Resource type	Catalyst 9500 High Perf	Catalyst 9500-X	Catalyst 9600	Catalyst 9600-X
Networking	AppGig Port	Mgmt Port*	2x10G	Mgmt Port*	Mgmt Port* (2x10G CPU ports)
Resources	Memory	8GB	8GB	8GB	8GB
	CPU	1 core	1 core	1 core	1 core
	Storage	Up to 960GB (SATA)	Up to 960GB (SATA)	Up to 960GB (SATA)	Up to 960GB (SATA)

* **Using** loopback with any external ports

Catalyst 9500-High Perf/X
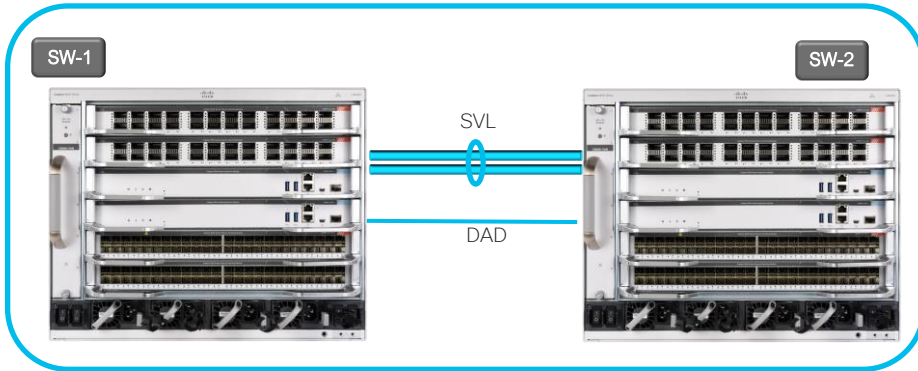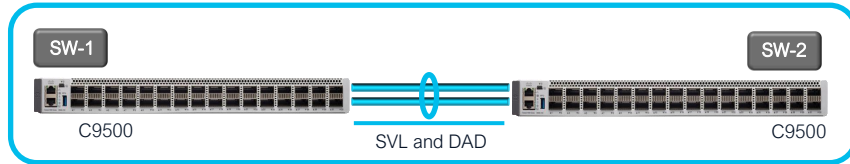
M2 SATA
Up to 90GB

Back panel

Catalyst 9600/X

M2 SATA
Up to 960GB

Plug into removable SUP

StackWise Virtual

SW-1   SW-2
C9500   C9500
SVL and DAD

SW-1   SW-2
SVL
DAD

- Supported on all the UADP base platform today
- Roadmap for the Silicon One ASIC platforms

- Simplify Operations by Eliminating STP, FHRP and Multiple Touch-Points

- Double Bandwidth & Reduce Latency with Active-Active Multi-chassis EtherChannel (MEC)

- Minimizes Convergence with Sub-second Stateful and Graceful Recovery (SSO/NSF)

Summary

The Catalyst 9000 Core and Dist Switches
Powering the cloud scale world

Cat 9500 / 9500X
Powered by UADP 3.0 / S1 Q200

NEW Catalyst 9500X
Powered by S1

100G/400G SKU's

Catalyst 9500
Powered by UADP 3.0

25G/100G SKU's

Catalyst 9600 / 9600X
Supervisor-1
Powered by UADP 3.0

Supervisor-2
Powered by S1 Q200

NEW

2.4Tbps Per Slot

6.4Tbps per Slot

NEW

Combo line cards

Fiber line cards
400G/100G/200G/50G/25G/10G/1G
- **40 x 50G/25G/10G/1G + 2 x 200G/100G + 2 x 400G**
- **32x 100G; or 28x 100G + 400G; or 24x 100G + 2x 400G**
- 24 x 100G / 40G
- 48 x 50G/25G/10G/1G
- 48 x 1G

Copper line card
- 48 x Mgig (Non-PoE)

Extending Core Leadership with Catalyst X Series

2.6x Bandwidth

WAN MacSec Support

400G Uplinks

2M Route Scale

Deep Buffers

Cisco Catalyst 9000 Core Series leadership

SD-Access

MACsec-256 link encryption

High Availability (SSO/ISSU)

Application Hosting

Model-driven programmability

Patching and GIR

Streaming telemetry

Simplicity with Open IOS-XE

Backward compatible for investment protection

Secure

Technical Session Surveys

- Attendees who fill out a minimum of four session surveys and the overall event survey will get Cisco Live branded socks!

- Attendees will also earn 100 points in the Cisco Live Game for every survey completed.

- These points help you get on the leaderboard and increase your chances of winning daily and grand prizes.

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Cisco U.
IT learning hub that guides teams and learners toward their goals

Cisco Digital Learning
Subscription-based product, technology, and certification training

Cisco Modeling Labs
Network simulation platform for design, testing, and troubleshooting

Cisco Learning Network
Resource community portal for certifications and learning

Train

Cisco Training Bootcamps
Intensive team & individual automation and technology training programs

Cisco Learning Partner Program
Authorized training partners supporting Cisco technology and career certifications

Cisco Instructor-led and Virtual Instructor-led training
Accelerated curriculum of product, technology, and certification courses

Certify

Cisco Certifications and Specialist Certifications
Award-winning certification program empowers students and IT Professionals to advance their technical careers
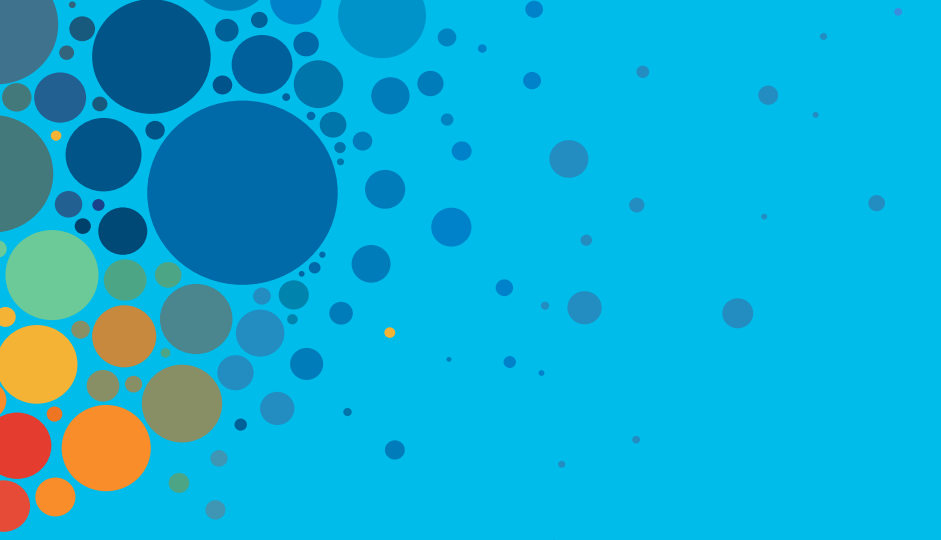
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Thank you